NCR 53C90A, 53C90B
Advanced SCSI Controller

General Description

The 53C90A and 53C90B are high performance CMOS devices conforming to the ANSI standard, X3.131-1986, for Small Computer Systems Interface (SCSI). They are a super-set of the 53C90 with additional commands and a second configuration register. The C90A is intended to directly replace a C90 in an existing design, allowing an easy upgrade to SCSI-2. The C90B has a parity pin on the host processor interface, but is otherwise identical to the C90A. Both are 100% compatible with existing 53C90 software.

The C90 family reduces protocol overhead by performing common SCSI algorithms, or sequences, in response to a single C90 command. The C90A and C90B will operate at sustained data transfer rates of 5 MB/S in synchronous mode and 5 MB/S in asynchronous mode. Refer to *Data Transfer Rate.*

Features

- ANSI X3.131-1986 compatible
- On-chip 48 mA drivers
- Control logic for differential tranceivers
- Parity generation, optional checking
- Parity pass through (53C90B only)
- Programmable transfer period
- Programmable offset
- SCSI-2 tagged-queing
- 16-byte FIFO
- 12 MB/S DMA interface
- Up to 5 MB/S asynchronous SCSI
- Up to 5 MB/S synchronous SCSI
- 25 MHz clock
- Low power CMOS
- 68-pin PLCC and 80-pin QFP

Figure 1. Functional Block Diagram

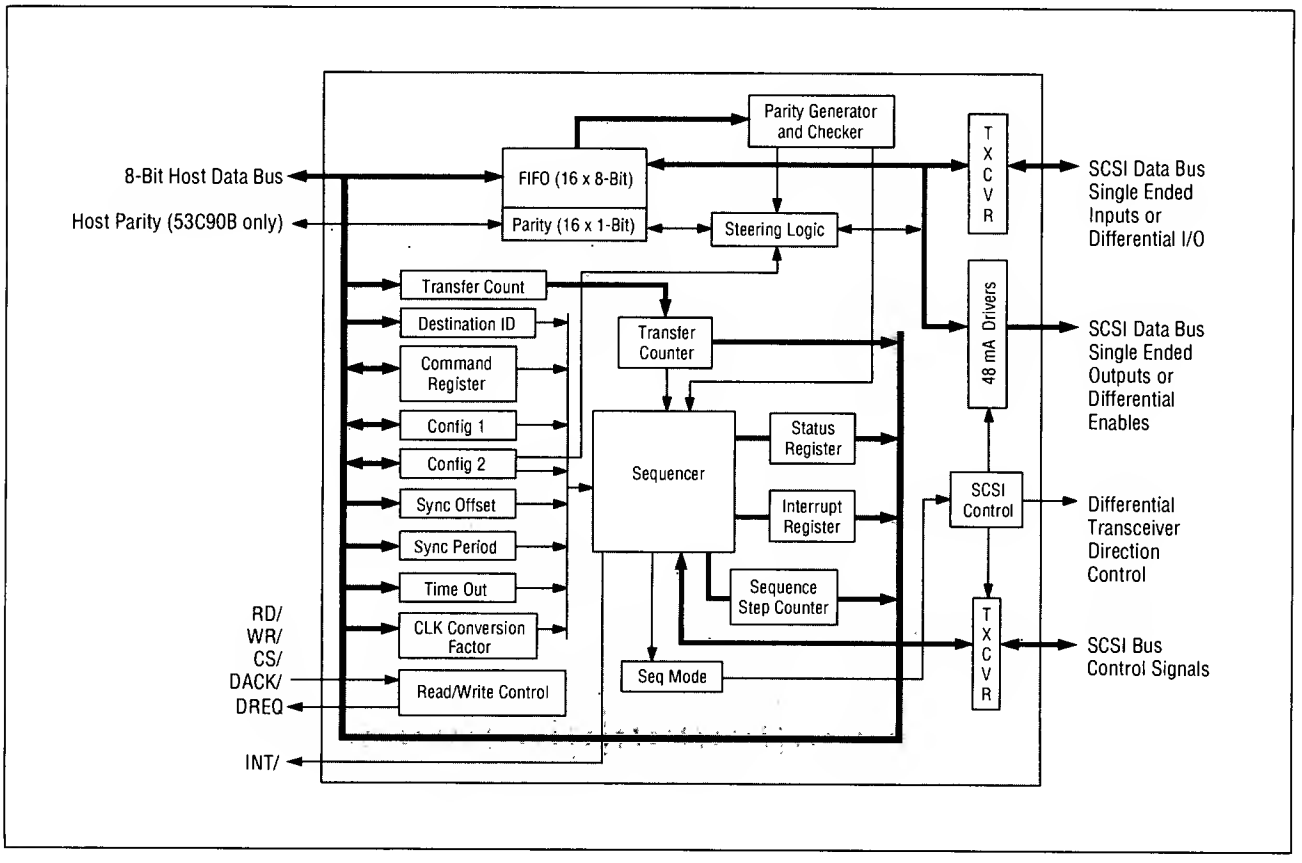


Figure 2. NCR 53C90 and 53C90A Pin Configurations

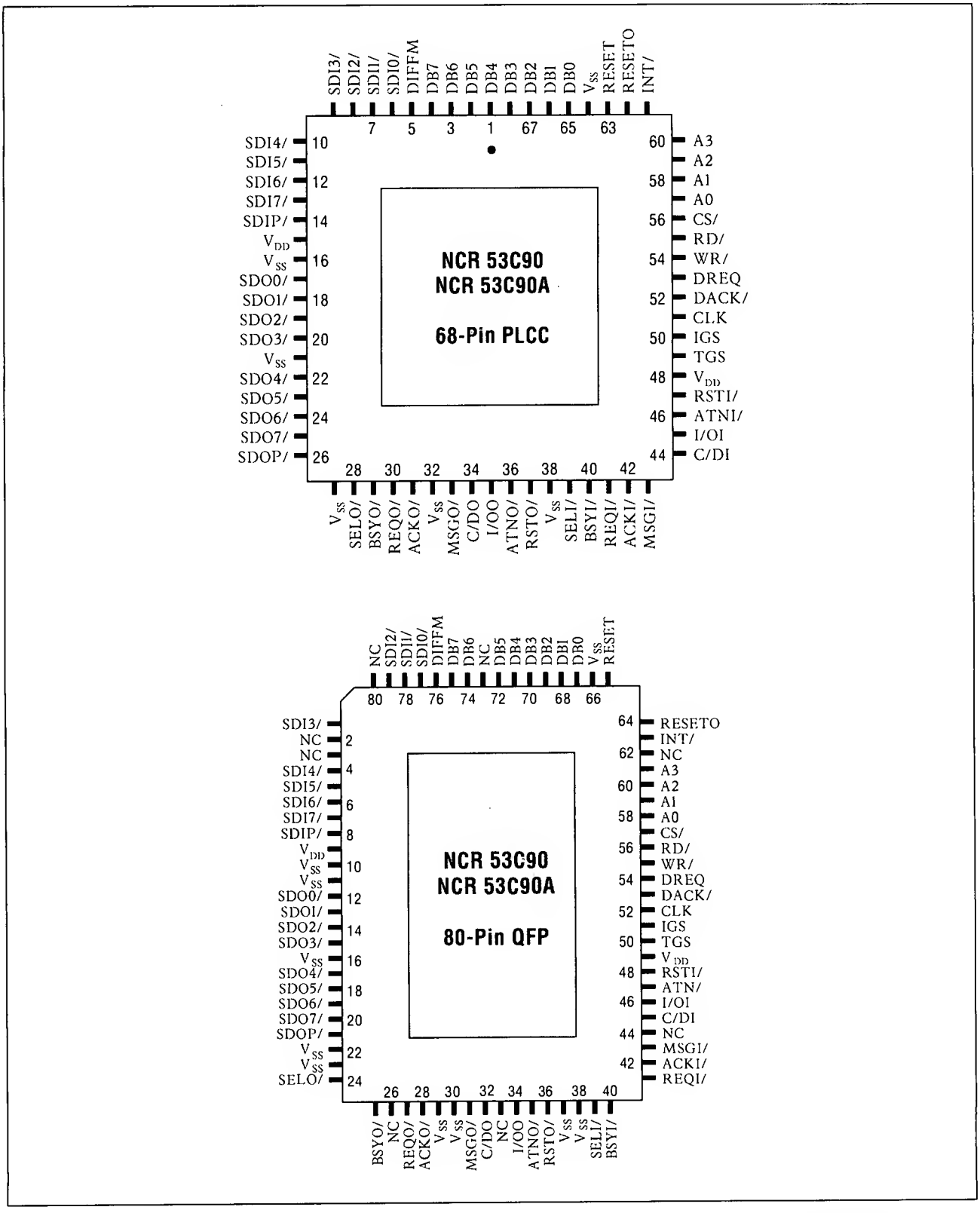


Figure 3. NCR 53C90B Pin Configurations

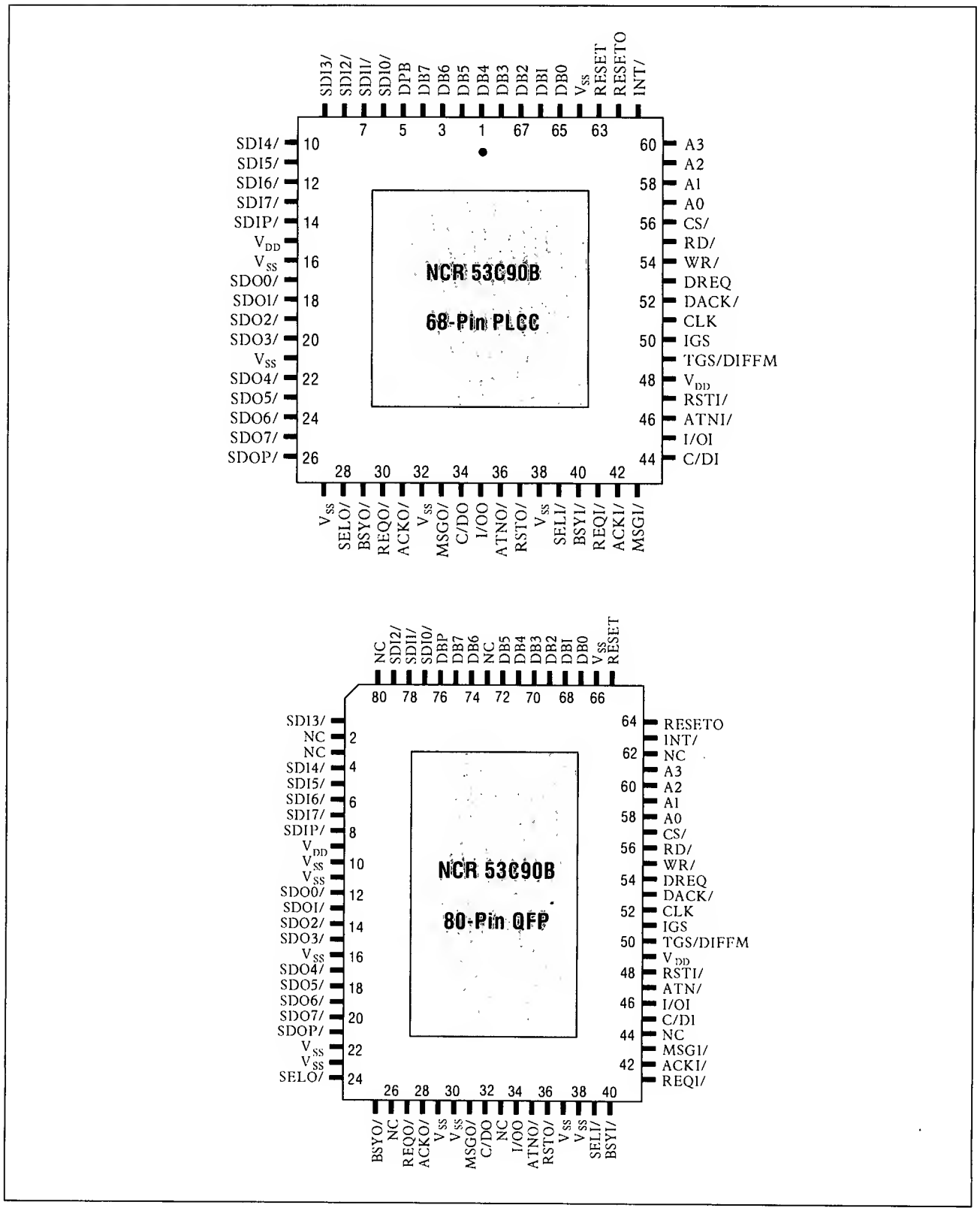


Table 1. Host Processor and DMA Interface Pins – PLCC Package

Pin	Signal	Type	Description
4-1, 68-65	DB7-DB0	B	Active-high data bus connected to the DMA controller, CPU and buffer memory. Each pad contains a pull-up to V_{DD} (12.5K minimum).
63	RESET	I	Active-high chip reset. Reset must be asserted for two CLK periods, mimimum, after the voltage on the power pins has reached V_{DD} min. This input must not be connected to RESETO.
62	RESETO	O	Active-high reset output. This output is always asserted when the RESET input is true OR may be asserted when the SCSI reset signal is active if bit 6 of the Config 1 register is cleared and the host has not serviced the interrupt (generated because of SCSI reset) within 1-2 ms (depending on CLK frequency and clock conversion factor). Refer to *Bus Initiated Reset.*
61	INT/	O	Active-low, open drain interrupt signal to the microprocessor. It is latched on the rising edge of CLK and may be cleared by reading the interrupt register or by a host hardware reset, or by a host software reset (but not by a SCSI reset). This output cannot be disabled internally.
60-57	A3-A0	I	Active-high address bus which specifies one of the ASPs internal registers for reading or writing. Used with CS/, ignored with DACK/.
56	CS/	I	Active-low chip-select signal that enables access to the ASPs internal registers. CS/ accesses any register, including the FIFO, while DACK/ accesses only the FIFO. CS/ and DACK/ must never be active at the same time.
55	RD/	I	Active-low read signal that enables ASP data onto DB7-DB0. CS/ or DACK/ must also be active.
54	WR/	I	Active-low write signal that strobes DB7-DB0 data into the ASP. CS/ or DACK/ must also be active.
53	DREQ	O	Tri-state active-high DMA request to the DMA controller. DREQ will be true as long as the FIFO has at least one byte to send to memory, or has room to receive at least one byte from memory, depending on data direction.
52	DACK/	I	Active-low DMA acknowledge from the DMA controller. DACK/ accesses the FIFO only, while CS/ accesses any register, including the FIFO. CS/ and DACK/ must never be active at the same time. DACK/ must toggle true then false for every byte transfered. Refer to *DREQ Hi Z Bit in Config 2.*
51	CLK	I	Square wave clock that generates internal chip timing. The maximum frequency is 25 MHz, with a 35% to 65% duty cycle. The minimum frequency required for asynchronous SCSI transmission is 10 MHz. The minimum frequency required for synchronous transmission is 12 MHz. The synchronous transmission rate is equal to the CLK input period divided by the value in the synchronous transfer period register. The asynchronous transfer rate is indirectly affected by CLK frequency. Refer to *Data Transfer Rate.*

Table 2. SCSI Bus Interface – PLCC Package

Pin	Signal	Type	Description
6-13, 14	SDI0/-SDI7/, SDIP/	B	Schmitt trigger, active-low SCSI data/parity bus. In single-ended mode (DIFFM = 0) these inputs are SCSI data bus signals. In differential mode (DIFFM = 1) these are bi-directional data and parity signals for external SCSI bus transceivers.
17-20, 22-25 26	SDO0/-SDO7/ SDOP	O O	48 mA, open drain SCSI data parity bus. In single-ended mode (DIFFM = 0) these outputs are active-low SCSI data signals. In differential mode (DIFFM = 1) these outputs are used to control the direction of external differential transceivers, with high meaning output to the SCSI bus, low meaning input from the SCSI bus.
28	SELO/	O	48 mA, open drain SCSI select signal. In single-ended mode this output is active-low. In differential mode it is active-high.
29	BSYO/	O	48 mA, open drain SCSI busy signal. In single-ended mode, this output is active-low. In differential mode it is active-high.
30	REQO/	O	48 mA, open drain, active-low SCSI request signal. This output is only asserted when the ASP is in target mode.
31	ACKO/	O	48 mA, open drain, active-low SCSI acknowledge signal. This output is only asserted when the ASP is in initiator mode.
33-35	MSGO/, C/DO, I/OO	O	48 mA, open drain, active-low SCSI phase signals. These outputs are only asserted when the ASP is in target mode.
36	ATNO/	O	48 mA, open drain, active-low SCSI attention signal. This output is only asserted when the ASP is in initiator mode. Several ASP commands will set ATN. It is also asserted when the ASP detects an incoming parity error if parity checking is enabled.
37	RSTO/	O	48 mA, open drain SCSI reset signal. In single-ended mode this output is active-low. In differential mode it is active-high. The ASP drives this signal true only when the host writes the SCSI bus reset command to the command register. The pulse length is 25-40 us, depending on CLK frequency and clock conversion factor. Refer to *Bus Initiated Reset*.
39	SELI/	I	Schmitt trigger, active-low SCSI select input.
40	BSYI/	I	Schmitt trigger, active-low SCSI busy input.
41	REQI/	I	Schmitt trigger, active-low SCSI request input.
42	ACKI/	I	Schmitt trigger, active-low SCSI acknowledge input.
43	MSGI/	I	Schmitt trigger, active-low SCSI message input.
44	C/DI	I	Schmitt trigger SCSI control/data input.
45	I/OI	I	Schmitt trigger SCSI input/output input.
46	ATNI/	I	Schmitt trigger, active-low SCSI attention input.
47	RSTI/	I	Schmitt trigger, active-low SCSI reset signal. When this input is true, the ASP will automatically disconnect from the SCSI bus. If bit 6 in the Config 1 register is zero, the ASP will interrupt the host. If the interrupt is not serviced within 1-2 ms, the ASP will reset its host processor. Refer to *Bus Initiated Reset*.
50	IGS	O	Active-high initiator group select signal. This pin is high whenever the ASP is in initiator mode. It is used in differential mode to enable the initiator signals (ACKO/, ATNO/). When low, the ASP should be receiving these signals.

Table 3. Power and Ground Pins

PLCC Pin Number	QFP Pin Number	Signal	Description
15, 48	9, 49	V_{DD}	+5 Volt power input.
16, 21, 27, 32, 38, 64	10, 11, 16, 22, 23, 29 30, 37, 66	V_{SS}	Ground. NCR recommends a ground plane be used.

Table 4. 53C90 and 53C90A only – PLCC Package

Pin	Signal	Type	Description
49	TGS	O	Active-high target group select signal. This pin is high whenever the ASP is in target mode. It is used in differential mode to enable the target signals (REQO/, MSGO/, C/DO, I/OO). When low, the ASP should be receiving these signals.
5	DIFFM	I	Differential mode enable. When this pin is grounded, the ASP operates in single-ended mode, with separate SCSI data input and output buses. When this pin is high, the ASP operates in differential mode, with bi-directional SCSI data on the SDI pins and active-high differential transceiver enables on the SDO pins.

Table 5. 53C90B only – PLCC Package

Pin	Signal	Type	Description
49	TGS/DIFFM	B	This pin is sampled during reset to put the chip in differential mode or single-ended mode, it then switches function to become the TGS output. An internal pull-up pulls it high for single-ended mode, while an external 1K pull-down will place the C90B in differential mode. There are two kinds of reset, power-up reset and running-reset. On power-up, the state of this pin is sampled as the voltage on the power pins rises through 3 volts (approximately). A running-reset is a host hardware reset that occurs sometime later. A running-reset will sample this pin until the 10th rising edge of CLK after RESET goes true (high). This is enough time for the internal pull-up to pull it high. Whatever state it's in on the 10th clock will determine the mode. The TGS function will be disabled until the 12th rising edge of CLK affer RESET first goes true and RESET is false. When RESET is false (low), and 12 clocks have occured since RESET first went true, this pin becomes the TGS output, an active-high target group select signal. This pin is high whenever the ASP is in target mode. It is used in differential mode to enable the target signals (REQO/, MSGO/, CDO/, IOO/). When low, the ASP should be receiving these signals.
5	DBP	B	Active-high data bus parity for host, DMA, and memory data bus. Four bits in Config 1 and Config 2 control parity generation and checking.

Differences from 53C90

- Supports three-byte message exchange SCSI-2 tagged-queuing
- Added select with ATN3 command
- Added target DMA abort command
- Added interrupt polling bit
- Added second configuration register
- Improved immunity to cable impedance mismatches and improper termination
- Tri-state DMA request output
- Cut leakage current on SCSI input pins when powered off
- Relaxed register timings
- Relaxed DMA timings
- Relaxed CLK duty cycle
- Lengthened read data access time
- NOP required less often

Functional Description

The ASC SCSI data bus has a set of inputs and a set of outputs. This allows the ASC to be used in either single-ended mode or differential mode. In single-ended mode, the inputs are usually connected to the outputs on the circuit board. In differential mode, the SDI (SCSI Data Input) pins become bi-directional data pins, while the SDO (SCSI Data Output) pins become enable signals for the differential transceivers. Separate enables are required, because during arbitration two data bus signals must be outputs while the other six must be inputs. Two signals, TGS and IGS, control the direction of the external transceivers, allowing the ASC to dynamically switch between initiator and target roles.

The ASC has a command set that allows it to perform common SCSI sequences at hardware speed without host intervention. Its on-chip FIFO may be accessed simultaneously by the SCSI bus and either the host processor or the host DMA controller. All command, data, status, and message bytes pass through the FIFO on their way to or from the SCSI bus. Most ASC commands have two versions: DMA and non-DMA. When DMA instructions are used, data will pass between memory and the SCSI bus with the FIFO acting as temporary storage when the DMA channel is temporarily shut down by a higher priority event such as DRAM refresh.

The FIFO also helps speed execution during non-DMA transfers. For example, in initiator role, the host processor will load the CDB (Command Descriptor Block) and optionally one or three message bytes into the FIFO, issue one of several selection commands and wait for an interrupt. The ASC will wait for bus-free, arbitrate for the bus again and again until it acquires it, send the message bytes followed by the CDB, then generate an interrupt. Meanwhile, a multi-tasking host may continue with other tasks.

In target role, the host processor will enable selection, then wait for an interrupt. Eventually, an initiator will select the ASC and will then automatically step through the arbitration, selection, and command phases before generating an interrupt. When the interrupt occurs, the entire command descriptor block will be in the FIFO along with any message bytes sent by the initiator. Combination commands such as these, are identified with the *sequence* suffix in the *Table of ASC Commands*.

After selection phase has been successfully completed, the ASC may transfer bytes in any of the SCSI information phases whether operating in initiator or a target role. The ASC supports disconnect/reselect in both initiator and target roles, making high performance multi-threaded systems easy to implement.

The ASC may transfer data phase bytes across the bus synchronously, at speeds up to 5 MB/S, or asynchronously at speeds up to 6 MB/S. Refer to *Data Transfer Rate*. The difference between the two is transparent to the user except that the synchronous offset and the synchronous transfer period registers must be programmed prior to synchronous data transfer. The default, after hardware or software reset, is asynchronous transmission.

Data phase bytes will usually be transferred using DMA. The host processor will program an external DMA controller, program the ASC transfer count, issue an ASC data transfer command (there are several), then wait for an interrupt. The DMA controller and the ASC will transfer all the data without host processor intervention.

To end the SCSI transaction, the ASC target will place a status byte and a message byte in the FIFO, then issue a single command (there are two to chose from) which will cause the ASC to first assert status phase, send the first byte, assert message in phase, send the second byte, disconnect from the SCSI bus (after the initiator releases ACK (Acknowledge)) and interrupt the host processor.

The end of a SCSI transaction is similar for an ASC initiator except that it receives two bytes into its FIFO. The initiator prevents the target from disconnecting by holding ACK asserted on the bus while the host processor examines the status and message bytes. If both bytes are good, the message accepted command is used to instruct the ASC to release ACK, which allows the target to disconnect which causes the initiator to interrupt its host and report the disconnect. If the status and message bytes are not good, the host should first issue the set ATN (Attention) command before issuing the message accepted command. This instructs the ASC to assert ATN before releasing ACK, which should cause the target to request message out phase rather than disconnect.

Bus Initiated Sequences

- Selection
- Reselection
- SCSI bus reset

Selection or reselection sequences occur in the disconnected state when the ASC is selected or reselected by another initiator or target, if the enable selection or reselection command had previously been received by the ASC.

In addition to responding to bus initiated events, the ASC may initiate a bus event by using one of several selection or reselection commands. If one of these commands starts executing, *it will clear enable selection/reselection* after arbitration has been won. Normally the host processor will have 250 ms (ANSI recommended selection time-out period) after the chip disconnects from the bus to re-enable bus initiated events. If the time-out is exceeded, an initiator or target which is attempting to connect to the ASC, may time-out and abort.

If, on the other hand, the bus initiated event occurs before the command starts executing, the FIFO and command register will be cleared, and any further writes by the host processor will be ignored until the interrupt register is read. Since a selection/reselection command requires that something be placed in the FIFO, these bytes will be lost, as will any command written to the command register. The interrupt handler that services a selection/reselection command will have to examine the bits in the interrupt register to detemine if the ASC selected another device, or if it was selected by another device. The former case will cause a function complete interrupt, the latter case will cause a selection/reselection interrupt.

Bus Initiated Selection

When the ASC has been selected as a target, the following data will be in its FIFO:

- Bus ID
- Identify message
- Command Descriptor Block (CDB)

The bus ID will always be present and will always be one byte. It is an un-encoded version of the state of the bus during selection phase. Any SCSI data bits that were true during selection phase will be set. The target ID (our ID) must always be set. In arbitrating systems, the initiator ID must also be set. The initiator ID is optional in non-arbitrating systems.

The identify message will always be present in the FIFO and will always be one byte in SCSI-1 systems but may be one or three bytes in SCSI-2 systems. If the initiator does not send an identify message (does not select with ATN), a null byte (00 hex) will be placed in the FIFO.

If the initiator selects with ATN and the SCSI-2 bit is cleared, the ASC target will request one message byte and will place it in the FIFO behind the bus ID. The ASC will then begin requesting command phase bytes unless the message byte is not a valid identify message, or a parity error is detected, which will cause the ASC to interrupt and stop. The sequence step register should then be examined.

If the initiator selects with ATN and the SCSI-2 bit is set, the ASC will examine both the message byte and the ATN signal to determine how many bytes to request. If the first byte is a valid identify message and if ATN goes false after receiving the first byte, the ASC will only request one message byte. If the first byte is a valid identify message byte and ATN is still true, it will request two more message bytes. The ASC will then begin requesting command phase bytes unless the first byte was not a valid identify message, or a parity error was detected, or ATN went false between the 2nd and 3rd bytes, or ATN remained true but the SCSI-2 bit was false, which will cause the ASC to interrupt and stop. The sequence step register should then be examined.

The Command Descriptor Block (CDB) will be placed in the FIFO behind the message byte(s), assuming selection completed normally. The CDB may be 6, 10 or 12 bytes long. Thus, in SCSI-2, the entire FIFO may be filled if a tagged-queue 12-byte command is used.

Bus Initiated Reselection

The ASC will allow itself to be reselected as an initiator by a target if it has previously received the enable selection/reselection command. If the sequence completes normally, the following information will be in the FIFO:

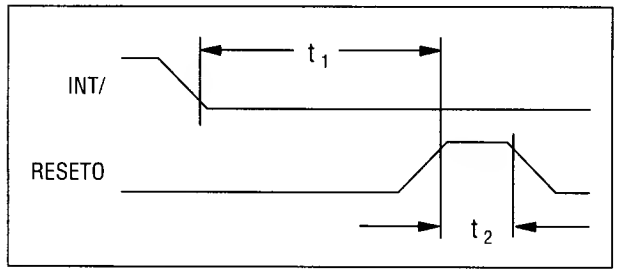
- Bus ID
- Identify message

The bus ID is the same as the selection case, described above. The identify message will always be present and always be one byte.

Bus Initiated Reset

A bus initiated reset will be recognized by the ASC at any time. The ASC will then disconnect from the bus and reset its internal sequencer. If the SCSI reset reporting bit (Config 1 register) is not set, the ASC will generate a SCSI reset detected interrupt. If the host processor does not read the interrupt register within t_1 milliseconds, the ASC will assert RESETO for t_2 microseconds.

Figure 4. Interrupt and Reset Timing



$t_1 = 2$ (CLK period)(3841CCF – 1)

$t_2 = 130$ (CLK period)(CCF)

Where CCF= Clock Conversion Factor
(Refer to *Description of Write Register 09*).

For example, at CLK= 25 MHz

$t_1 = 1.5$ milliseconds

$t_2 = 26$ microseconds

Data Transfer Rate

Performance claims for the ASC are based on it being directly connected to the SCSI bus with no external transceivers. In differential mode, external transceivers are required and will slow asynchronous transmission by the propagation delay of the chosen transceiver but will not slow synchronous transmission.

The synchronous data transmission rate is equal to the CLK input frequency divided by the encoded value in the synchronous period register. Sustained synchronous transfer rates of 5 MB/S are attainable across the commercial voltage and temperature range.

The asynchronous transmission rate will vary with cable length and the CLK period. The ASC can reach sustained transfer rates of 6 MB/S on short (one-foot) cables using typical devices operating at or near nominal voltage and temperature. The worst case asynchronous transmission rate over voltage, temperature, and process variations is 3 MB/S on a maximum length (single-ended) cable and 4.5 MB/S on a one-foot cable.

The asynchronous transmission rate is only slightly affected by the CLK frequency when sending data. The ASC will drive the data bus for a minimum of one CLK period before asserting REQ or ACK. The CLK frequency does not affect the asynchronous transfer rate when receiving data.

Table 6. ASC Register Set

Address (hex)	Read	Write
0	Transfer counter LSB	Transfer count LSB
1	Transfer counter MSB	Transfer count MSB
2	FIFO	FIFO
3	Command	Command
4	Status	Destination bus ID
5	Interrupt	Select/reselect timeout
6	Sequence step	Synchronous period
7	FIFO flags/sequence step	Synchronous offset
8	Configuration 1	Configuration 1
9	NCR reserved	Clock conversion factor
A	NCR reserved	Test mode
B	Configuration 2	Configuration 2

Register Set

Some ASC registers have different meanings during reads than writes. When CS/ is true, the register being accessed is determined by either RD/ or WR/ together with the address pins A0-3. The FIFO may be accessed using either CS/ or DACK/ together with RD/ or WR/. Address pins A0-A3 are ignored when DACK/ is active, but must be driven when CS/ is active.

Transfer Count (Write address 0,1)

These two registers together form a 16-bit transfer count for DMA operations. Transfer count specifies the number of bytes that are to be transferred over the SCSI bus. Values written to these two registers will be stored internally and loaded into the transfer counter by any DMA command. These values remain unchanged while the transfer counter decrements. Thus, successive blocks of equal size may be transferred without reprogramming the count. They may be reprogrammed any time after the previous DMA operation has started, whether it has finished or not. Zero specifies a maximum length count (65536). These registers are not changed by any reset; their states are unpredictable after power-up .

Transfer Counter (Read address 0,1)

A read from these two addresses will return the value currently in the counter. DMA commands use the counter to terminate a transfer. Any DMA command will load count into the counter. A DMA NOP 80h will load the counter while the non-DMA NOP 00h will not.

With one exception, non-DMA commands do not use the counter. The exception is when the ASC has been selected, it decodes the group code field of the CDB (Command Descriptor Block), loads the counter with the number of bytes in the CDB, then decrements once for every byte received.

The transfer counter decrements on the leading edge of:

Target	Decremented by
Data in phase	DACK/
Data out phase	REQO/

Initiator	Decremented by
Synchronous data in	DACK/
Asynchronous data in	ACKO/
Data out	DACK/

Note that DACK/ can decrement the counter even if RD/ or WR/ do not go true. False DACK/s can cause the counter to get out of sync with the data stream, leading to subtle errors that are difficult to trace. When false DACK/s are expected to interfere with a temporarily suspended DMA operation, the DREQ Hi-Z bit in Config 2 should be set.

FIFO Register (Read/write address 02)

The FIFO is a 16 by 9-bit first-in-first-out buffer between the SCSI bus and memory. It is accessible by the host processor at this address. It is also accessible by an external DMA controller and by the SCSI bus. The DMA may access the FIFO by asserting DACK/ together with either RD/ or WR/. When accessed by CS/, the address bits must be valid. When accessed by DACK/, the address bits are ignored. The bottom FIFO element and the FIFO flags are initialized to zero during hardware reset, software reset chip and at the beginning of bus initiated selection or reselection. The contents of the rest of the FIFO are not changed by any reset, but when the flags are zero, successive FIFO reads will always access the bottom register.

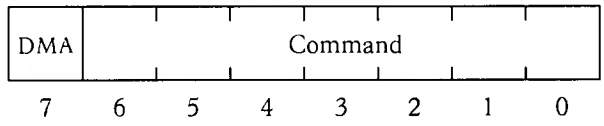
Command Register (Read/write address 03)

The command register is a two deep 8-bit read/write register used to give commands to the ASC. Up to two commands may be stacked in the command register. The second command may be written before the ASC completes (or even starts) the first. Reset chip, reset SCSI bus and target stop DMA execute immediately, all others wait for the previous command to complete. The last executed (or executing) command will remain in the command register and may be read by the host processor. Reading the command register has no effect on its contents. The command register will be cleared by any of the following conditions:

- Hardware, software or SCSI bus reset
- SCSI bus disconnect
- Bus-initiated selection or reselection
- Select command
- Reconnect command if ATN is set
- Select or reselect time-out
- Target terminate command
- Parity error detected in target mode
- Assertion of ATN in target mode
- Any phase change in initiator mode
- Illegal command

If two commands are placed in the command register, two interrupts may result. If the first interrupt is not serviced before the second finishes, the second interrupt is stacked behind the first. When the interrupt register is read by the host to service the first interrupt, the contents status register, sequence step register, and interrupt register will change to describe the second interrupt.

Figure 5. Command Register (Read/write address 03)



Bit 7 (Enable DMA)

When bit 7 is not set, the command is a non-DMA instruction. When it is set, the command is a DMA instruction. DMA instructions will load the internal byte counter with the value in the transfer count register (without changing the count register) then transfer data until that count decrements to zero. If the transfer terminates prematurely, the bits in the status , sequence step, and interrupt registers will indicate why.

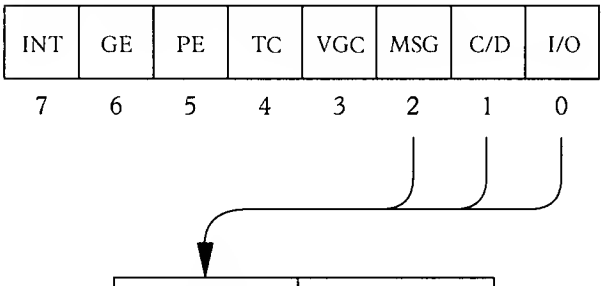
Bits 6-0 (Command code)

The ASC commands are shown in *Table 19*. Bits 4, 5 and 6 specify a mode group. Commands from the miscellaneous group may be issued at any time. Commands from the disconnected, target or initiator groups will only be accepted by the ASC if it is in the same mode as the command when it falls to the bottom of the command FIFO. Otherwise, an illegal command interrupt will be generated. For example, after hardware or software reset, the ASC will be in the disconnected state. A command from either the target group or the initiator group will cause an illegal command interrupt. An enable selection or reselection command by itself will not change modes. However, if another SCSI device then selects the ASC, it will be in the target state; if another device reselects the ASC, it will then be in the initiator state. Similarly, any select command will place the ASC in initiator mode, while the reselect sequence command will place the ASC in target mode.

Status Register (Read address 04)

The satus register contains important flags that indicate various conditions. All but the phase bits are latched. The phase bits are live indicators of the state of the SCSI bus. All the latched bits except the terminal count are cleared by reading the interrupt register.

Figure 6. Status Register (Read address 04)



Bits 2	1	0	SCSI Phase
0	0	0	Data out
0	0	1	Data in
0	1	0	Command
0	1	1	Status
1	0	0	ANSI reserved
1	0	1	ANSI reserved
1	1	0	Message out
1	1	1	Message in

Bit 7 (Interrupt)
This bit is set whenever the ASC drives the INT output true. It may be polled. It is buffered from the actual output, so that in wired-OR (shared interrupt) designs, this bit will indicate whether the ASC is attempting to interrupt the host processor. This bit is reserved by NCR in the 53C90. Hardware reset or software reset chip or a read from the interrupt register will release an active INT signal and also clear this bit.

Bit 6 (Gross error)
This bit is set when one of the following has occurred:

- The top of the FIFO is overwritten
- The top of the command register has been overwritten
- Direction of DMA transfer is opposite to the direction of the SCSI transfer
- An unexpected phase change in initiator role during synchronous data phase

Gross error does not cause an interrupt, it may be detected only while servicing another interrupt. The bit is cleared by reading the status register if the interrupt output is asserted. It will also be cleared by hardware reset, or software reset chip (but not SCSI reset).

Bit 5 (Parity error)
This bit will be set if parity checking is enabled in the Config 1 register and the ASC detects a SCSI parity error on incoming command, data, status or message bytes. It will be cleared by reading the interrupt register if the interrupt output is asserted. Hardware reset or software reset chip will clear this bit (but not SCSI reset).

Bit 4 (Terminal count)
This bit is set when when the transfer counter decrements to zero. It resets when the transfer count is loaded. Since a DMA NOP 80h command will load the transfer counter, it will also clear this bit. Note that a non-DMA NOP 00h will not load the counter and will not clear this bit. Reading the interrupt register will not clear this bit. Hardware reset or software reset chip will clear it (but not SCSI reset).

Bit 3 (Valid group code)
The name of this bit has changed from transfer complete in the 53C90 to valid group code in the 53C90A and 53C90B; but it's function remains the same.

When the ASC is selected, it decodes the group code field in the first byte of the command descriptor block. If the group code matches one defined in ANSI X3.131-1986, this bit will be set. An undefined group code (designated reserved by the ANSI committee) leaves it not set. If the SCSI-2 bit is set in the Config 2 register, group 2 commands will be recognized as ten-byte commands and the bit will be set. If the SCSI-2 bit is cleared, group 2 commands will be treated as reserved commands. Groups 3 and 4 are always treated as reserved commands. A reserved group command will cause the ASC to request 6 command bytes. The ASC recognizes group 6 as six-byte vendor unique commands and group 7 as 10-byte vendor unique commands. The valid group code bit will be cleared by reading the interrupt register if the interrupt output is asserted. It will also be cleared by hardware reset or software reset chip (but not by SCSI reset).

Bits 2-0 (Phase bits)
These bits indicate the phase on the SCSI bus at the time the register was read. These bits are live, if the phase changes, so will these bits. In target role, the ASC is driving these lines so they will not change if the read follows an interrupt. In initiator role, the ASC will generate its interrupt only after the target asserts REQ (Request). The ANSI specification requires that the phase lines be valid before asserting REQ and remain valid until the initiator asserts ACK(Anowledge). Thus, these bits can be expected to be stable during any read that follows an interrupt.

Destination ID (Write address 04)

The least significant 3 bits of this register specify the encoded destination bus ID for a selection or reselection command. These bits are binary encoded, with 111 representing device ID 7, which appears as 80h on the SCSI bus. The most significant 5 bits are reserved by NCR. The destination ID is not changed by any reset, the states of these bits are unpredictable after power-up.

Interrupt Register (Read address 05)

This 8-bit register is used in conjunction with the status register and sequence step register to determine the cause of an interrupt. Reading this register when the interrupt output is true will clear all three registers. The entire interrupt register will be cleared (0) by hardware reset or software reset chip (but not SCSI reset).

Figure 7. Interrupt Register (Read address 05)

SCSI RST	Ill CMD	Dis	BS	FC	Re SEL	SEL ATN	SEL
7	6	5	4	3	2	1	0

Bit 7 (SCSI reset detected)
This bit is set if the SCSI reset reporting bit in the Config 1 register is set to zero and the chip detects a reset on the SCSI bus.

Bit 6 (Illegal command)
This bit is set when an unused code is placed in the command register or when the command is from a mode group different than the mode the ASC is currently in. Refer to the *Command Register* definition.

Bit 5 (Disconnect)
In initiator mode, this bit is set when the target disconnects or a selection or reselection time-out occurs. When the ASC is in target mode, this bit is set if a terminate sequence or command complete sequence command causes the ASC to disconnect from the bus.

Bit 4 (Bus service)
This bit indicates that another device is requesting service. In target mode, it is set whenever the initiator asserts ATN (Attention).

In initiator mode, it is set whenever the target is requesting an information transfer phase.

Bit 3 (Function complete)
This bit will be set after any target mode command has completed. In initiator mode, it is set after a target has been selected (before transferring any command phase bytes), after command complete finishes, or after a transfer info command when the target is requesting message in phase.

Bit 2 (Reselected)
This bit is set during reselection phase to indicate that the ASC has been reselected as an initiator.

Bit 1 (Selected with ATN)
This bit is set during selection phase to indicate that the ASC has been selected as a target and that ATN was asserted on the SCSI bus.

Bit 0 (Selected)
This bit is set during selection phase to indicate that the ASC has been selected as a target and that ATN was false during selection.

Time-Out (Write address 05)

This 8-bit write-only register specifies the amount of time to wait for a response during selection or reselection. (The ASC has no way to time-out if it never wins arbitration, it will keep trying indefinitely until it wins). The time-out register is normally loaded to specify a time-out period of 250 ms. The Register Value (RV) may be calculated from:

$$RV = \frac{\text{(Time-out period) (CLK frequency)}}{\text{8192 (Clock conversion factor)}}$$

For example, at 25 MHz, the register value that gives a 250 ms time-out period is 153 decimal or 99 hexadecimal. The clock conversion factor is defined in the description of write address 9. The time-out register remains unchanged by any reset, the states of these bits are unpredictable after power-up.

Synchronous Transfer Period (Write address 6)

The lower five bits of this register specify the minimum time between leading edges of successive REQ (Request) or ACK(Acknowledge) pulses. Synchronous data will be transmitted or received at the rate of one byte every N clocks (CLK). N is related to the register value as shown below.

Register Value	Clocks per Byte
0 0 1 0 0	5
0 0 1 0 1	5
0 0 1 1 0	6
0 0 1 1 1	7
-	-
-	-
-	-
1 1 1 1 1	31
0 0 0 0 0	32
0 0 0 0 1	33
0 0 0 1 0	34
0 0 0 1 1	35

Missing entries in the table above follow the binary code. The upper three bits are reserved by NCR. This register defaults to 5 after hardware reset or software reset chip (but not SCSI reset).

Sequence Step (Read address 06)

The lower 3 bits of this register are used to indicate how far the internal sequencer was able to proceed in executing combination commands. This counter will be incremented at certain points in various algorithms to aid in error recovery if the previous command does not complete normally.

Table 7. Initiator Select with ATN and Stop

Sequence Step	Interrupt Register	Interpretation
2 1 0	7 6 5 4 3 2 1 0	
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; selection time-out; disconnected
0 0 0	0 0 0 1 1 0 0 0	Arbitration and selection complete; stopped because target did not assert message out phase; ATN still asserted by ASC
0 0 1	0 0 0 1 1 0 0 0	Message out complete; sent one message byte; ATN on

Table 8. Initiator Select without ATN

Sequence Step	Interrupt Register	Interpretation
2 1 0	7 6 5 4 3 2 1 0	
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; selection time-out; disconnected
0 1 0	0 0 0 1 1 0 0 0	Arbitration and selection complete; stopped because target did not assert command phase
0 1 1	0 0 0 1 1 0 0 0	Stopped during command transfer because target prematurely changed phase
1 0 0	0 0 0 1 1 0 0 0	Select sequence complete

Table 9. Initiator Select with ATN

Sequence Step	Interrupt Register	Interpretation
2 1 0	7 6 5 4 3 2 1 0	
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; selection time-out; disconnected
0 0 0	0 0 0 1 1 0 0 0	Arbitration and selection complete; stopped because target did not assert message out phase; ATN still driven by ASC
0 1 0	0 0 0 1 1 0 0 0	Message out complete; sent one message byte with ATN true, then released ATN; stopped because target did not assert command phase after message byte was sent
0 1 1	0 0 0 1 1 0 0 0	Stopped during command transfer due to premature phase change; some CDB bytes may not have been sent; check FIFO flags
1 0 0	0 0 0 1 1 0 0 0	Selection with ATN sequence complete

Table 10. Initiator Select with ATN3

Sequence Step	Interrupt Register	Interpretation
2 1 0	7 6 5 4 3 2 1 0	
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; selection time-out; disconnected
0 0 0	0 0 0 1 1 0 0 0	Arbitration and selection complete; stopped because target did not assert message out phase; ATN still driven by ASC
0 1 0	0 0 0 1 1 0 0 0	Sent 1, 2, or 3 message bytes; stopped because target prematurely changed from message out phase or did not assert command phase after third message byte; ATN released only if third message byte was sent
0 1 1	0 0 0 1 1 0 0 0	Stopped during command transfer due to premature phase change; Some CDB bytes may not have been sent; check FIFO flags
1 0 0	0 0 0 1 1 0 0 0	Selection with ATN3 sequence complete

Table 11. Target Selected without ATN

Sequence Step	Interrupt Register	Interpretation
2 1 0	7 6 5 4 3 2 1 0	
0 0 0	0 0 0 0 0 0 0 1	Selected, loaded bus ID into FIFO, loaded null-byte message into FIFO
0 0 1	0 0 0 0 0 0 0 1	Stopped in command phase due to parity error; some command descriptor block bytes may not have been received; check FIFO flags
0 0 1	0 0 0 1 0 0 0 1	Same as above, initiator asserted ATN in command phase
0 1 0	0 0 0 0 0 0 0 1	Selected, received entire command descriptor block; check valid group status bit
0 1 0	0 0 0 1 0 0 0 1	Same as above, initiator asserted ATN in command phase

Table 12. Target Selected with ATN SCSI-2 Bit Not Set

Sequence Step	Interrupt Register	Interpretation
2 1 0	**7 6 5 4 3 2 1 0**	
0 0 0	0 0 0 0 0 0 1 0	Selected with ATN, stored bus ID and one message byte; stopped due either to parity error or invalid ID message
0 0 0	0 0 0 1 0 0 1 0	Selected with ATN, stored bus ID and one message byte; stopped because ATN remained true after lst message byte
0 0 1	0 0 0 0 0 0 1 0	Stopped in command phase due to parity error; some CDB bytes not received; check valid group code bit and FIFO flags
0 0 1	0 0 0 1 0 0 1 0	Stopped in command phase; parity error and ATN true
0 1 0	0 0 0 0 0 0 1 0	Selection complete; received one message byte and the entire command descriptor block
0 1 0	0 0 0 1 0 0 1 0	Same as above, initiator asserted ATN during command phase

Table 13. Target Selected with ATN SCSI-2 Bit Set

Sequence Step	Interrupt Register	Interpretation
2 1 0	**7 6 5 4 3 2 1 0**	
0 0 0	0 0 0 0 0 0 1 0	Selected with ATN, stored bus ID and one message byte; stopped due either to parity error or invalid ID message
1 0 0	0 0 0 0 0 0 1 0	Parity error during second or third message byte
1 0 0	0 0 0 1 0 0 1 0	ATN remained true after third message byte
1 0 1	0 0 0 0 0 0 1 0	Received 3 message bytes; then stopped in command phase due to parity error; some CDB bytes not received; check valid group code bit and FIFO flags
1 0 1	0 0 0 1 0 0 1 0	Stopped in command phase; parity error and ATN true
1 1 0	0 0 0 0 0 0 1 0	Selection complete; received 3 message bytes and the entire command descriptor block

Table 14. Target Receive Command

Sequence Step	Interrupt Register	Interpretation
2 1 0	**7 6 5 4 3 2 1 0**	
0 0 1	0 0 0 0 1 0 0 0	Stopped during command transfer due to parity error; check FIFO flags
0 0 1	0 0 0 1 1 0 0 0	Stopped during command transfer due to parity error; ATN asserted by initiator
0 1 0	0 0 0 0 1 0 0 0	Received entire command descriptor block
0 1 0	0 0 0 1 1 0 0 0	Received entire CDB, initiator asserted ATN

Table 15. Target Disconnect Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	**7 6 5 4 3 2 1 0**	
0 0 0	0 0 0 1 1 0 0 0	Sent one message byte; stopped because initiator set ATN
0 0 1	0 0 0 1 1 0 0 0	Sent two message bytes; stopped because initiator set ATN
0 1 0	0 0 1 0 1 0 0 0	Disconnect sequence complete; disconnected; bus is free

Table 16. Target Terminate Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	**7 6 5 4 3 2 1 0**	
0 0 0	0 0 0 1 1 0 0 0	Sent status byte; stopped because initiator set ATN
0 0 1	0 0 0 1 1 0 0 0	Sent status and message bytes; stopped because initiator set ATN
0 1 0	0 0 1 0 1 0 0 0	Terminate sequence complete; disconnected; bus is free

Table 17. Target Command Complete Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	**7 6 5 4 3 2 1 0**	
0 0 0	0 0 0 1 1 0 0 0	Sent status byte; stopped because initiator set ATN
0 0 1	0 0 0 1 1 0 0 0	Sent status and message bytes; stopped because initiator set ATN
0 1 0	0 0 0 0 1 0 0 0	Command complete sequence complete

FIFO Flags (Read address 07)

The least significant five bits of this register indicate how many bytes are currently in the FIFO. The value is binary encoded. The flags should not be polled while transferring data because they will not be stable while the SCSI interface is changing the contents of the FIFO.

Figure 8. FIFO Flags (Read address 07)

SS2	SSI	SS0	FF4	FF3	FF2	FFI	FF0
7	6	5	4	3	2	1	0

SS = Sequence Step *FF = FIFO Flag*

The upper three bits are duplicates of the sequence step register bits when operating in normal mode.

If test mode is enabled, bit 5 is set to indicate that the offset counter is not zero. Not zero means that synchronous data may continue to be transferred. Zero means that the synchronous offset count has expired and the ASC will not transfer any more data until it receives an acknowledge.

Synchronous Offset (Write address 07)

The least significant four bits of this register specify whether the ASC will transfer data phase bytes synchronously or asynchronously. *Zero specifies asynchronous transfer.* Any other value specifies the synchronous offset; the number of data phase bytes that may be sent synchronously without an acknowledge (either REQ or ACK), depending on whether the ASC is in initiator or target mode).

When transmitting to the SCSI bus, the ASC will stop sending bytes when it reaches this offset and, thereafter, send one byte for every acknowledge it receives from the other SCSI device.

When receiving from the SCSI bus, the ASC will send an acknowledge every time a byte is removed from its FIFO on the DMA (or host processor) interface. The maximum offset of I5 allows a receiving ASC to store data in its FIFO while the external DMA controller gains control of the memory bus.

The synchronous offset is cleared (0) by hardware reset or software reset chip (but not SCSI reset).

Configuration 1 Register (Config 1) (Read/write address 08)

This 8-bit read/write register specifies various operating conditions for the ASC. Any bit pattern written to this register may be read back and should be identical.

Figure 9. Configuration 1 Register (Config 1) (Read/write address 08)

Slow	$\overline{\text{SRR}}$	P Test	En P Chk	Chip Test	My Bus ID		
7	6	5	4	3	2	1	0

Bit 7 (Slow cable mode)
Slow cable mode will seldom be necessary. It compensates for excessive capacitive loading on the SCSI data signals by inserting an extra CLK period between data being asserted on the bus and REQ or ACK being driven true. This bit is cleared (0) by hardware reset or software reset chip (but not SCSI reset).

Bit 6 (SCSI Reset Reporting Interrupt Disable)
This bit disables the reporting of a SCSI reset. If the SCSI reset signal goes true when this bit is set, the ASC will disconnect from the SCSI bus and remain idle in the disconnected state without interrupting the host. If the bit is not set, the ASC will respond to the SCSI reset by first interrupting the host, then resetting the host if the interrupt is not serviced within 1-2 ms (depending on CLK frequency and clock conversion factor.) Refer to *Bus Initiated Reset.* This bit is cleared (0) by hardware reset or software reset chip (but not SCSI reset).

Bit 5 (Parity test mode)
Setting this bit will cause the parity signal to be a duplicate of data bit 7 when unloading the FIFO to either the SCSI bus or the host processor bus (53C90B only). This allows parity errors to be created so that hardware and software may be tested. This bit must not be set during normal operation. Refer to *Parity Checking and Generation.* This bit is cleared (0) by hardware reset or software reset chip (but not SCSI reset).

Bit 4
When this bit is set, the ASC will check parity on incoming SCSI bytes during any information transfer phase except when receiving bad bytes. Detected parity errors will cause a bit to be set in the status register but will

not cause an interrupt. In initiator role, bad parity will also set ATN (Attention) on the SCSI bus. When this bit is not set, parity will not be checked; the bit in the status register will not be set, and ATN will not be asserted. Refer to *Parity Checking and Generation.* This bit is cleared (0) by hardware reset or software reset chip (but not SCSI reset).

Bit 3 (Chip test mode enable)
When this bit is set, the chip is placed in special test mode that enables the test register at address 0Ah. Once it has been set, the chip must be reset (hard or soft but not SCSI) before normal operation can begin. This bit should not be set during normal operation. This bit is cleared (0) by hardware reset or software reset chip (but not SCSI reset).

Bit 2-0 (My bus ID)
This bitfield is the bus ID of this device. It is the ID to which the ASC responds during bus initiated selection or reselection, and the ID that the ASC uses to arbitrate for the bus. The name of this field has changed from bus ID on the C90, but its function remains the same. This three bit field is binary encoded. These bits are cleared by a hardware reset or software reset command (but not SCSI reset).

Clock Conversion (Write address 09)

This register must be set according to the CLK (clock) input frequency. All timings longer than 400 ns depend on this register correctly agreeing with the CLK frequency. The least significant three bits are binary encoded, and should be set to one of the four values below.

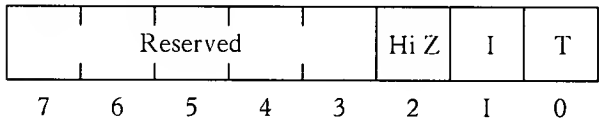
CLK Frequency (MHz)	Clock Conversion Factor
I0	2
10.0I to 15	3
I5.0I to 20	4
20.0I to 25	5

This register must never be loaded with I. Hardware reset or software reset chip will set the clock conversion register to 2. SCSI reset will not affect it. The upper 5 bits of this register are reserved by NCR.

Test Register (Write address 0A)

This register is enabled by setting the special test mode bit in config-I at address 08. After test mode has been entered, a hardware reset or software reset chip must occur before normal operation can begin.

Figure 10. Test Register (Write address 0A)



Bit 2 (All outputs to high-impedance)
When this bit is set, all bi-directional and all output pins go to high-impedance and will not significantly load a TTL or compatible device.

Bit 1 (Initiator mode)
When this bit is set, the ASC is artificially forced into initiator mode. Any initiator command will be accepted by the ASC. For example, a set ATN command will cause ATN to be driven on the SCSI bus even if the ASC is disconnected.

Bit 0 (Target mode)
When this bit is set, the ASC is artificially forced into target mode. Any target command will be accepted by the ASC. For example, a DMA command will load or unload the FIFO and set the SCSI phase, data and REQ signals even if arbitration and selection have not occurred.

Configuration 2 (Config 2) (Read/write address 0B)

The 53C90A and 90B have a second configuration register that did not exist in the original C90. After hardware reset or software reset chip, the bits in this register are all cleared, which makes the chip compatible with the older 53C90. Any bit pattern written to this register may be read back and should be identical.

Figure 11. Configuration 2 (Config 2) (Read/write address 0B)

Reserved			DREQ Hi Z	SCSI 2	BPA	RPE	DPE
7	6	5	4	3	2	1	0

Bit 4 (DREQ high-impedance)
When this bit is set, the DREQ output (DMA Request) goes to high impedance and will not significantly load a TTL compatible device. This is useful when several devices share the DMA request line (known as wired-OR). When this bit is set, the ASC will ignore any activity on the DACK/ (DMA Acknowledge) input.

When this bit is cleared, the DREQ output will be driven to TTL high or low voltages. When this bit is cleared, DACK/ is enabled to decrement the transfer counter and load or unload the FIFO, depending or WR/ or RD/. DACK/ should not pulse true without RD/ or WR/ because the transfer counter may decrement without transferring any data. Refer to *Transfer Counter Register*.

Bit 3 (SCSI-2)
Allows the ASC to support two new features adopted in SCSI-2: the three-byte message exchange for tagged-queuing and group 2 commands.

Tagged-Queuing
When this bit is set, and the ASC is selected with ATN (Attention), it will request either one or three message bytes depending on whether ATN remains true or goes false. If ATN is still true after the first byte has been received, the ASC may request two more message bytes before switching to command phase. If ATN goes false, it will request only one message byte then switch to command phase. When the bit is not set it will request a single message byte (as a target) when selected with ATN; and abort the selection sequence (as an initiator) if the target does not switch to command phase after one message byte has been transferred. Refer to *Bus Initiated Selection.*

Group 2 Commands
When the SCSI-2 bit is set, group 2 commands are recognized as 10-byte commands. Receiving a group 2 command with this bit set will set the valid group code bit in the status register. If the SCSI-2 bit is not set the ASC will treat group 2 commands as reserved commands, it will request only 6 bytes in command phase and will not set the valid group code status bit.

Bit 2 (Target bad parity abort)
When this bit is set, the ASC will abort a receive command or receive data sequence when the ASC detects a parity error.

Bit 1 (Register parity enable)
When this bit is set, parity from the host DBP pin (53C90B only) will be loaded into the FIFO when CS/ and WR/ are both true. When this bit is not set the ASC generates parity from the host data bus when CS/ and WR/ are both true and places it in the FIFO along with the data from which it was generated.

When the ASC is moving data from the FIFO to the SCSI bus, it will flag outgoing parity errors if either this bit or the DMA parity enable bit is set.

Bit 0 (DMA parity enable)
When this bit is set, parity from the host DBP pin (53C90B only) will be loaded into the FIFO when DACK/ and WR/ are both true. When this bit is not set, the ASC generates parity from the host data bus when DACK/ and WR/ are both true and places it in the FIFO along with the data from which is was generated.

When the ASC is moving data from the FIFO to the SCSI bus, it will flag outgoing parity errors if either this bit or the register parity enable bit are set.

Table 18. Parity Control

Control Bit	Data Direction	Bit Set	Bit Not Set
Parity checking Config 1, bit 4	SCSI to FIFO	Enable parity checking and error reporting. SDPB loaded into FIFO.	Disable parity checking and error reporting. Parity generator to FIFO.
Test parity Config 1, bit 5	FIFO to SCSI	SDBP is replica of SDB7	FIFO to SDBP
	FIFO to host	DBP is replica of DB7	FIFO to DBP
DMA parity Config 2, bit 0	DACK/ to FIFO	DBP to FIFO	Parity generator to FIFO
	FIFO to SCSI	Enable parity checking and error reporting	Disable parity checking and error reporting
Register parity Config 2, bit 1	CS/ to FIFO	DBP to FIFO	Parity generator to FIFO
	FIFO to SCSI	Enable parity checking and error reporting	Disable parity checking and error reporting

Parity Checking and Generation

The ASC has four bits that control parity generation and checking. If parity checking is disabled, the ASC does not check for parity errors. In this document, the word *detected,* in conjunction with *parity error,* should be understood to imply that parity checking has previously been enabled. In target role, detected parity errors will set the parity error status bit and clear the command register. In initiator role, detected parity errors will set the parity error bit and assert ATN (Attention) prior to releasing ACK(Acknowledge). Parity errors occurring on the first few bytes after a phase change to synchronous data in are handled slightly differently in initiator mode. Refer to *Initiator Commands.*

If parity test mode is enabled, the parity bit is a duplicate of bit 7. This is true both for data flowing from the FIFO to the SCSI Data Bus (SDB) or data flowing from the FIFO to the Host Data Bus (DB).

The 53C90B has a parity pin (DBP) on the host bus. It may pass parity between SCSI and host buses without changing it or flagging errors; or may generate parity from the data byte. Whether generated internally or externally, the parity bit is always loaded into the FIFO along with the data byte. From there on it moves through the FIFO along with the byte. The FIFO may be accessed by three busses: SCSI bus, host processor bus, or host DMA bus.

When checking parity, the ASC checks "at the edge of the board." Parity errors are flagged as data comes into the FIFO from the SCSI bus, or as it leaves the FIFO on its way out to the SCSI bus.

Table 19. ASC Command Set

Command Register								Command Mnemonic	Interrupt
7	6	5	4	3	2	1	0		
								Miscellaneous Group	
X	0	0	0	0	0	0	0	NOP	No
X	0	0	0	0	0	0	1	Flush FIFO	No
X	0	0	0	0	0	1	0	Reset chip	No
X	0	0	0	0	0	1	1	Reset SCSI bus	No *
								Disconnected State Group	
X	1	0	0	0	0	0	0	Reselect sequence	Yes
X	1	0	0	0	0	0	1	Select without ATN sequence	Yes
X	1	0	0	0	0	1	0	Select with ATN sequence	Yes
X	1	0	0	0	0	1	1	Select with ATN and stop sequence	Yes
X	1	0	0	0	1	0	0	Enable selection/reselection	No
X	1	0	0	0	1	0	1	Disable selection/reselection	Yes
X	1	0	0	0	1	1	0	Select with ATN3	Yes
								Target State Group	
X	0	1	0	0	0	0	0	Send message	Yes
X	0	1	0	0	0	0	1	Send status	Yes
X	0	1	0	0	0	1	0	Send data	Yes
X	0	1	0	0	0	1	1	Disconnect sequence	Yes
X	0	1	0	0	1	0	0	Terminate sequence	Yes
X	0	1	0	0	1	0	1	Target command complete sequence	Yes
X	0	1	0	0	1	1	1	Disconnect	No
X	0	1	0	1	0	0	0	Receive message	Yes
X	0	1	0	1	0	0	1	Receive command sequence	Yes
X	0	1	0	1	0	1	0	Receive data	Yes
X	0	1	0	1	0	1	1	Receive command sequence	Yes
X	0	0	0	0	1	0	0	Target abort DMA	No **
								Initiator State Group	
X	0	0	1	0	0	0	0	Transfer information	Yes
X	0	0	1	0	0	0	1	Initiator command complete sequence	Yes
X	0	0	1	0	0	1	0	Message accepted	Yes
X	0	0	1	1	0	0	0	Transfer pad	Yes
X	0	0	1	1	0	1	0	Set ATN	No
X	0	0	1	1	0	1	1	Reset ATN	No

* *The command itself does not cause an interrupt, however, external connection of the RSTO/ pin to RSTI/ pin causes an interrupt if the SCSI reset reporting is not disabled in the configuration register.*

** *The command itself does not cause an interrupt, however, it may allow a stalled command to finish and generate an interrupt.*

Command Set

From the programmers point of view, DMA commands will move data between memory and the SCSI bus, non DMA commands will move data between the FIFO and the SCSI bus. Non-DMA commands require the host processor to move data between the FIFO and memory. DMA commands require an external DMA controller to move data between the FIFO and memory. A command with bit 7 set is a DMA command. A command with bit 7 not set is a non-DMA command. DMA commands will load the transfer counter with whatever value is in the transfer count register, so the value must be correct before issuing the command.

Table 20. Miscellaneous Commands

DMA	Non-DMA	Mnemonic
80	00	No-Operation (NOP)
81	01	Flush FIFO
82	02	Reset chip
83	03	Reset SCSI bus

Miscellaneous Commands

NOP

No-Operation. The 53C90A and 53C90B require this command only after hardware reset or software reset chip. A DMA NOP 80h may be used to load the transfer counter with the value in transfer count register. No interrupt is generated from this command.

Flush FIFO

The Flush FIFO command initializes the FIFO to the empty condition by resetting the FIFO flags and setting the bottom byte of the FIFO to zero.

Reset Chip

This command resets all functions in the chip and returns it to a disconnected state. The command has the same effect as a hardware reset, with the exception that reset chip cannot change between single-ended mode or differential mode.

Reset SCSI Bus

This command will assert the SCSI Reset Output (RSTO) signal for 25 µs, depending on CLK frequency and clock conversion factor. Refer to *Bus Initiated Reset*. This command does not cause an interrupt; however, since RSTI will be externally connected to RSTO, an interrupt will be generated unless it is disabled in the Config 1 register.

Table 21. Disconnected State Commands

DMA	Non-DMA	Mnemonic
C0	40	Reselect sequence
C1	41	Select without ATN sequence
C2	42	Select with ATN sequence
C3	43	Select with ATN and stop sequence
C4	44	Enable selection or reselection
C5	45	Disable selection and reselection
C6	46	Select with ATN3

Disconnected State Commands

If any of the Disconnected State commands are received by the ASC when it is not in the disconnected state, the command will be ignored, the command register will be cleared, and the ASC will generate an illegal command interrupt.

Reselect Sequence

This command will cause the ASC target to arbitrate for the bus then enter reselection phase when it wins arbitration. The identify message, required by SCSI protocol, must either be placed in the FIFO by the host processor before issuing the command or must be transfenred by DMA, which involves setting the transfer count to one and setting up the external DMA controller. In either case, the time-out and destination ID must have previously been set. The sequence will terminate early if a reselect time-out occurs.

Select without ATN Sequence

This command will cause the ASC initiator to arbitrate for the bus, enter selection phase when it wins, and send the CDB (Command Descriptor Block). The 6, 10, or 12 byte CDB must have either been placed in the FIFO previously by the host processor or must be transferred by DMA, which involves setting the transfer count to 6, 10 or 12 and programming the external DMA controller. In either case, the time-out and destination registers must have previously been set. This command terminates early if a reselection time-out occurs, or the target does not assert command phase, or the target removes command phase too early. If it terminates normally, a function complete/bus service interrupt will be generated.

Select with ATN Sequence

This command will cause the ASC initiator to arbitrate for the bus, select a device with ATN true then send one message phase byte followed by 6, 10 or 12 command phase bytes. The message and command bytes must have either been placed in the FIFO by the host processor or must be transferred by DMA, which involves setting the transfer count to 7, 11 or 13 and programming the external DMA controller. In either case, the time-out and destination ID registers must have previously been programmed. This command terminates early if: a select time-out occurs, target does not assert message phase followed by command phase, or target removes command phase early. If it completes normally, a function complete and bus service interrupt will be generated.

Select with ATN and Stop

This command should be used in place of the one above when multiple message phase bytes are to be sent. The command will select a target with ATN asserted, send one message phase byte, and generate a bus service interrupt and stop.

Enable Selection/Reselection

After receiving this command, the ASC will respond to bus initiated selection or reselection. A command that causes the ASC to select or reselect will cancel this command. The command must be re-issued within 250 ms after the ASC disconnects to preserve ANSI recommended timings. If DMA is enabled, incoming Command Descriptor Block will be placed in memory. If DMA is not enabled, incoming information will remain in the FIFO.

Disable Selection/Reselection

This command disables an earlier Enable Selection/ Reselection command. If bus initiated selection or reselection had not yet begun when this command is received by the ASC, it will generate a function complete interrupt. If bus initiated selection or reselection had already begun, this command (and every other command) will be ignored. Refer to *Bus Initiated Selection* and *Bus Initiated Reselection*.

Select with ATN3 Sequence

This command is similar to the select with ATN command, but sends three message bytes instead of one. It will cause the ASC initiator to arbitrate for the bus, select a device with ATN true, send three message phase bytes, deassert ATN, then send 6, 10, or 12 command phase bytes. The message and command bytes must have either been placed in the FIFO by the host processor or must be transferred by DMA; this involves setting the transfer count to 7, 11, or 13 and programming the external DMA controller. In either case, the time-out and destination ID registers must have previously been programmed. This command terminates early if: a select time-out occurs, target does not assert message phase followed by command phase or target removes command phase early. If it completes normally, a function complete and bus service interrupt will be generated.

Table 22. Initiator Commands

DMA	Non-DMA	Mnemonic
90	10	Transfer information
91	11	Initiator command complete sequence
92	12	Message accepted
98	18	Transfer pad
9A	1A	Set ATN (Attention)
-	1B	Reset ATN (Attention)

Initiator Commands

If the ASC is not in initiator state when it receives any of these commands, the command will be ignored, an illegal command interrupt will be generated, and the command register will be cleared. Refer to *Command Register.*

If BSY goes false while the ASC is connected as an initiator, it will generate a disconnected interrupt. The interrupt output will occur 1.5 to 3.5 CLK cycles after BSY goes false.

When the ASC receives the last byte of a message in phase, it will leave ACK (Acknowledge) asserted on the bus to prevent the target from sending any more bytes until the initiator decides to accept or reject the message. For non-DMA commands, every byte is presumed to be the last byte. For DMA commands, the transfer counter signals the last byte.

If parity checking is enabled and the ASC detects a parity error while in initiator mode, it will automatically assert ATN prior to deasserting ACK for the byte which has the error. The one exception is after a phase change to synchronous data in, described below.

If the synchronous offset register is non-zero (synchronous) and the phase changes to data in, the DMA interface is immediately disabled and the reporting of a parity error during data in phase is delayed. The phase, change to data, in will: latch the FIFO flags to indicate how many bytes were in the FIFO (these bytes will be lost), clear the FIFO, load the FIFO with the first data in byte, generate an interrupt, and continue to load the FIFO with incoming data in bytes as long as the target sends them, but not more than the specified offset. To continue receiving data in bytes, the host processor would normally issue the transfer information command to re-enable the DMA interface. If parity checking is enabled, and a parity error occurred on a previous input phase (message in or status), then the parity error flag will be set in the status register, and ATN (Attention) will be set on the SCSI bus. If a parity error occurred during the data in phase, the parity bit will not be set, nor will ATN be asserted until after the ASC receives the subsequent transfer information command.

Transfer Information

This command can be used to send or receive any information phase bytes, but is most often used for data transfer. For synchronous transfer, DMA must be used. The ASC will continue to transfer information until one of the following terminating events occurs:

- Transfer is complete. This successful completion will create a bus service interrupt. For a DMA transfer info, the transfer is complete when the transfer count decrements to zero and the FIFO is empty and the target asserts REQ (Request) for the next byte. For non-DMA transfer info in which the ASC is sending bytes to the SCSI bus, transfer is complete when the FIFO empties and the target asserts REQ for the next byte. For non-DMA transfer info in which the ASC is receiving bytes from the SCSI bus, transfer is complete after one byte is received and the target asserts REQ for the next byte. Thus, non-DMA transfer info commands will generate an interrupt for every byte received.

  If the phase is message out, the ASC removes ATN prior to asserting ACK for the last byte of the message. For non-DMA, every byte is assumed to be the last byte. For DMA, the transfer counter indicates the last byte.

- Target changes phase. The ASC clears the command register and generates a bus service interrupt, after the target asserts REQ for the next byte.

- Target releases BSY (Busy). The ASC generates a disconnected interrupt.

- The ASC receives the last byte of a message in phase. (For non-DMA every byte is assumed to be the last byte. For DMA, the transfer counter signals the last byte.) The ASC leaves ACK(Acknowledge) asserted and generates a function complete interrupt.

  All message in and status phase transfers are handled one byte at a time. If DMA is enabled, the next byte will not be received until the current byte has been written to buffer memory and the FIFO is empty. If DMA is not enabled, each byte will create an interrupt.

Initiator Command Complete Sequence

This command will cause the ASC to receive a status byte followed by a message byte. It terminates early if the target does not assert message in phase, or if the target disconnects. After receiving the message byte, the ASC leaves ACK asserted on the bus to allow the initiator to assert ATN if the message is unacceptable.

Message Accepted

This command releases the ACK signal on the SCSI bus. Any of the commands that receive bytes during message phase will leave ACK asserted after receiving the last message byte. To accept the message, issue this command. To reject the message, set ATN, then issue this command.

Transfer Pad

Transfer Pad is usually an error recovery technique. It is useful when a target requests more bytes than an initiator has to send, or when an initiator must receive and discard a number of bytes from a target.

When transmitting to the SCSI bus, Transfer Pad will fill the FIFO with null bytes and send them to the SCSI bus. When receiving from the SCSI bus, Transfer Pad will receive bytes, place them on the top of the FIFO and discard them from the bottom of the FIFO.

When sending pad bytes to the SCSI bus, DMA must be enabled. No DMA requests are actually made, but the ASC uses the transfer counter to end the transfer.

The command terminates under the same conditions as the transfer info command, except that the ASC does not leave ACK asserted on the last byte of a message in phase. If the command terminates early (due to phase change or disconnect) the FIFO may contain bad bytes.

Set ATN

This command asserts attention on the SCSI bus. No interrupt is generated from this command. ATN stays asserted until the last byte of a message out phase. DMA commands use the transfer counter to indicate the last byte. For non-DMA commands, every byte is assumed to be the last byte. ATN will also be released if the target prematurely disconnects.

Reset ATN

This command causes ATN to be released. It does not cause an interrupt.

This command must not be used when connected to a device supporting the Common Command Set (CCS). The ASC obeys CCS protocol by releasing ATN on the last byte of a message out phase. The Reset ATN command is provided for older devices that do not respond properly to the ATN condition.

Table 23. Target Commands

DMA	Non-DMA	Mnemonic
A0	20	Send message
A1	21	Send status
A2	22	Send data
A3	23	Disconnect sequence
A4	24	Terminage sequence
A5	25	Target command complete sequence
A7	27	Disconnect
A8	28	Receive message sequence
A9	29	Receive command
AA	2A	Receive data
AB	2B	Receive command sequence
84	04	Target abort DMA

Target Commands

If the ASC receives any of these commands when it is not in target state, it will ignore the command, clear the command register, and generate an illegal command interrupt. Refer to *Command Register*.

Normal completion of these commands will cause a function complete interrupt. If ATN is asserted, the bus service bit will be set in the status register. If the ASC was idle when ATN was asserted, a bus service interrupt will be generated, the function complete bit will be zero, and the command register will be cleared.

Send Message

This command will cause the ASC to assert message in phase and send bytes until the FIFO is empty and the transfer counter is zero (if DMA).

Send Status

This command will cause the ASC to assert status phase and send bytes until the FIFO is empty and the transfer counter is zero (if DMA).

Send Data

This command will cause the ASC to assert data in phase and send bytes until the FIFO is empty and the transfer counter is zero (if DMA).

Disconnect Sequence

This command will cause the ASC to assert message in phase, send two bytes, then disconnect from the SCSI bus. Normally, the first byte will be a save data pointers message and the second will be a disconnect message. If ATN is asserted by the initiator, the bus service and function complete bits will be set; an interrupt will be generated, but the ASC will not disconnect.

Terminate Sequence

This command will cause the ASC to first assert status phase, send one byte; then assert message in phase and send one more byte. If ATN is asserted by the initiator, the bus service and function complete bits will be set, an interrupt will be generated, but the ASC will not disconnect.

Target Command Complete Sequence

This command is similar to terminate sequence, but is used for linked commands. It will cause the ASC to first assert status phase, send one byte, then assert message in phase and send one more byte. The message byte will normally be a command complete message. If ATN is asserted by the initiator, the bus service and function complete bits will be set; an interrupt will be generated, but the ASC will not disconnect.

Disconnect

This command causes the ASC to release all SCSI bus signals except RSTO. The ASC returns to the disconnected state without generating an interrupt.

Receive Command

This command will cause the ASC to assert command phase and receive bytes from the initiator. For non-DMA Receive command, only one byte per interrupt may be received. DMA Receive command will interrupt after the transfer counter decrements to zero.

Receive Data

This command will cause the ASC to assert data out phase and receive bytes from the initiator. For non-DMA Receive Data, only one byte per interrupt may be received. DMA Receive Data will interrupt after the transfer counter decrements to zero.

Receive Command Sequence

This command will cause the ASC to assert command phase and receive a number of bytes, which will vary according to the the group code field of the first byte. If the SCSI-2 bit is set in the Config 2 register, group 2 commands will be recognized as 10-byte commands. If the SCSI-2 bit is cleared, group 2 commands will be recognized as reserved commands. groups 3 and 4 are always reserved. The ASC will request 6 bytes for reserved commands, 6 bytes for group 6 vendor unique commands, and 10 bytes for group 7 vendor unique commands.

Target Stop DMA

This command allows the host processor to stop a DMA data transfer command. The ASC must be in target state when this command falls to the bottom of the command FIFO or an illegal command interrupt will be generated. Target stop DMA may only be used when all of the following are true.

1) Either a Target Send Data or Target Receive Data command are currently executing.

2) The DMA controller has stopped.

3) The ASC is in *steady state*, that is:
   a) Send data – the FIFO is empty.
   b) Receive asynchronous data – the FIFO is full or the transfer counter is zero.
   c) Receive sync data – the transfer counter is zero or the synchronous offset max bit (read register 06, bit 3) is not set.

Upon receiving this command, the ASC will reset the DMA interface (release DREQ) then terminate the current command. It will not generate its interrupt until the rest of the completion criteria are met.

1) Send asynchronous data – completes immediately.

2) Send synchronous data – completes when the offset counter is zero.

3) Receive asynchronous data – completes immediately. There will be data in the FIFO which should be removed by the host processor.

4) Receive synchronous data – completes when all outstanding SCSI ACKs have been received. The offset counter is separate from the transfer counter. There will be data in the FIFO which should be removed by the host processor.

DC Electrical Characteristics

Absolute Maximum Stress Ratings

Parameter	Symbol	Pins	Test Conditions	Min	Max	Unit
Storage temperature	T_{STG}	-	-	−55	150	°C
Supply voltage	V_{DD}	-	-	−0.5	7.0	V
Input voltage	V_{IN}	-	-	V_{SS}−0.5	V_{DD}+0.5	V
Latch-up current	I_{LP}	-	$-2V < V_{PIN} < +8V$	±100	-	mA
Electrostatic discharge	ESD	-	Human body model	-	-	-
		SCSI pins	100 pF at 1.5K ohms	±6000	-	V
		Other pins	100 pF at 1.5K ohms	±3000	-	V

Conditions that exceed the absolute maximum stress limits may destroy the device.

Conditions that exceed the operating limits may cause the device to function incorrectly.

Operating Conditions

Parameter	Symbol	Pins	Test Conditions	Min	Max	Unit
Supply voltage	V_{DD}	-	-	4.75	5.25	V
Supply current	I_{DD}	-	Static*	-	10	mA
Supply current	I_{DD}	-	Dynamic	-	50	mA
Ambient temperature	T_A	-	-	0	70	°C

* *Static means: all inputs at V_{SS}, all outputs floating, and all bi-directional pins configured as inputs.*

Inputs

Parameter	Symbol	Pins	Test Conditions	Min	Max	Unit
Input high voltage	V_{IH}	-	-	2.0	V_{DD} + 0.5	V
Input low voltage	V_{IL}	-	-	V_{SS} − 0.5	0.8	V
Input leakage current	I_{IN}	Non-SCSI	$0 < V_{IN} < V_{DD}$ $4.75 \le V_{DD} \le 5.25$	−10	10	µA
Hysteresis	V_H	BSYI/, SELI/, REQI/,ACKI/, RSTI/	-	400	-	mV
Input low leakage	I_{IL}	SCSI	$V_{IN} = 0.5; 0 \le V_{DD} \le 5.5$	−10	0.0	µA
Input high leakage	I_{IH}	SCSI	$V_{IN} = 2.7; 0 \le V_{DD} \le 5.5$	0.0	10	µA
Capacitance	C_{IN}	-	-	-	10	pF

Outputs

Parameter	Symbol	Pins	Test Conditions	Min	Max	Unit
Output high voltage	V_{OH}	DREQ, IGS,	I_{OH}= −2 mA	2.4	V_{DD}	V
Output low voltage	V_{OL}	DREQ, IGS, INT/	I_{OL}= 4 mA	V_{SS}	0.4	V
Output high voltage	V_{OH}	RESTO	I_{OH}= −4 mA	2.4	V_{DD}	V
Output low voltage	V_{OL}	RSTO/, SELO, ATNO/, MSGO/, ACKO/, REQO/, SDOP/, BSYO/, C/D, I/O, SDO7-0	I_{OL}= 48 mA	V_{SS}	0.5	V
Hi Z state leakage	I_{OZ}	-	$0 < V_{OUT} < V_{DD}$	−10	10	µA
Capacitance	C_{OUT}	-	-	-	10	pF

Bi-Directional Pins

Parameter	Symbol	Pins	Test Conditions	Min	Max	Unit
Input high voltage	V_{IH}	-	-	2.0	V_{DD}+ 0.5	V
Input low voltage	V_{IL}	-	-	V_{SS}−0.5	0.8	V
Output high voltage	V_{OH}	SDI7-0, DBI5-0, DBPI-0, PAD7-0	I_{OH}= −2 mA	2.4	V_{DD}	V
Output low voltage	V_{OL}	SDI7-0, DBI5-0, DBPI-0, PAD7-0	I_{OL}= 4 mA	V_{SS}	0.4	V
Output high voltage	V_{OH}	TGS	I_{OH}= −4 mA	2.4	V_{DD}	V
Output low voltage	V_{OL}	TGS	I_{OL}= −8 mA	V_{SS}	0.4	V
Input current, low	I_{IL}	TGS	-	−600	0	µA
Input current, low	I_{IN}	SDI7-0	$0 < V_{IN} < V_{DD}$	−10	10	µA
Input current, low	I_{IL}	DBI5-0, DBPI-0, PAD7-0	V_{IN}= V_{IL}	−400	0	µA
Input current, high	I_{IH}	DBI5-0, DBPI-0, PAD7-0, TGS	V_{IN}= V_{IH}	0	I0	µA
Hi Z pull-up current	I_{PU}	DBI5-0, DBPI-0, PAD7-0	-	I00	400	µA
Capacitance	C_{IO}	-	-	-	10	pF

AC Electrical Characteristics

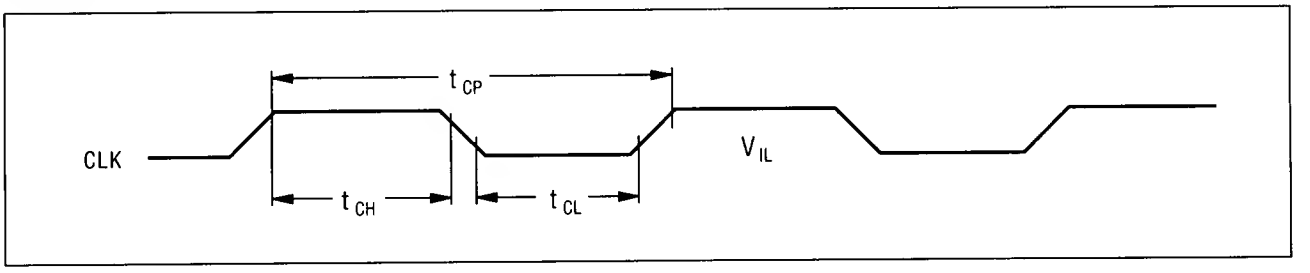
The AC characteristics described herein apply over the voltage range V_{DD}= 4.75 - 5.25 V and the temperature range 0°-70°C. Chip output timing is based on simulation under worst case conditions (4.75 V, 70°C) and the following pad termination:

Signal Name	Output Load
RESETO, DREQ, TGS, IGS, SDIP/, SDI7/-SDI0/	50 pF
DB7-0	85 pF
INT/	50 pF, IK pull-up
RSTO/, SELO/, BSYO/, ATNO/, MSGO/, CDO/ IOO/, REQO/, ACKO/, SDO7-0/, SDOP	200 pF, I10 pullup, 165 pulldown

System Interface

All timings in this specification are taken from the I0% and 90% points with respect to the specified V_{OL} and V_{OH} of the waveforms.

Clock

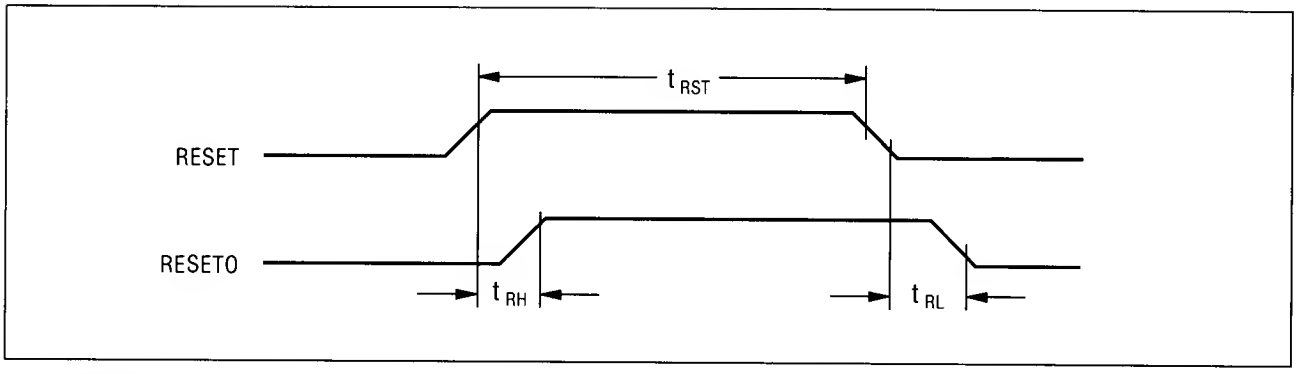


Parameter	Symbol	Minimum	Maximum	Units
Clock period	t_{CP}	40	I00	ns
Clock frequency, asynchronous	t_{CPA}	10*	25	MHz
Clock frequency, synchronous	t_{CPS}	I2*	25	MHz
Clock high	t_{CH}	14.58	-	ns
Clock low	t_{CL}	14.58	-	ns
Synchronization latency = $t_{CP} + t_{CL}$	t_{CS}	-	-	-

* *These minimum numbers required to comply with ANSI SCSI specification. For synchronous SCSI data transfers, the clock inputs must also meet the following requirements:*

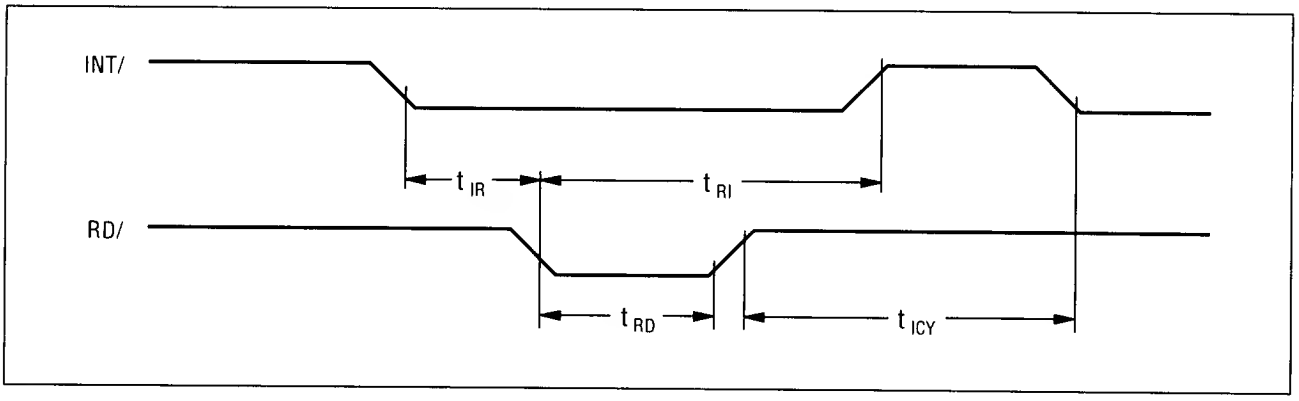
$2t_{CP} + t_{CL} \geq 97.92$ ns and $2t_{CP} + t_{CH} \geq 97.92$ ns

Reset Input



Parameter	Symbol	Minimum	Maximum	Units
RESET pulse width	t_{RST}	$2\,t_{CP}$	-	ns
RESET high to RESETO high	t_{RH}	-	50	ns
RESET low to RESETO low	t_{RL}	-	50	ns

Interrupt Output

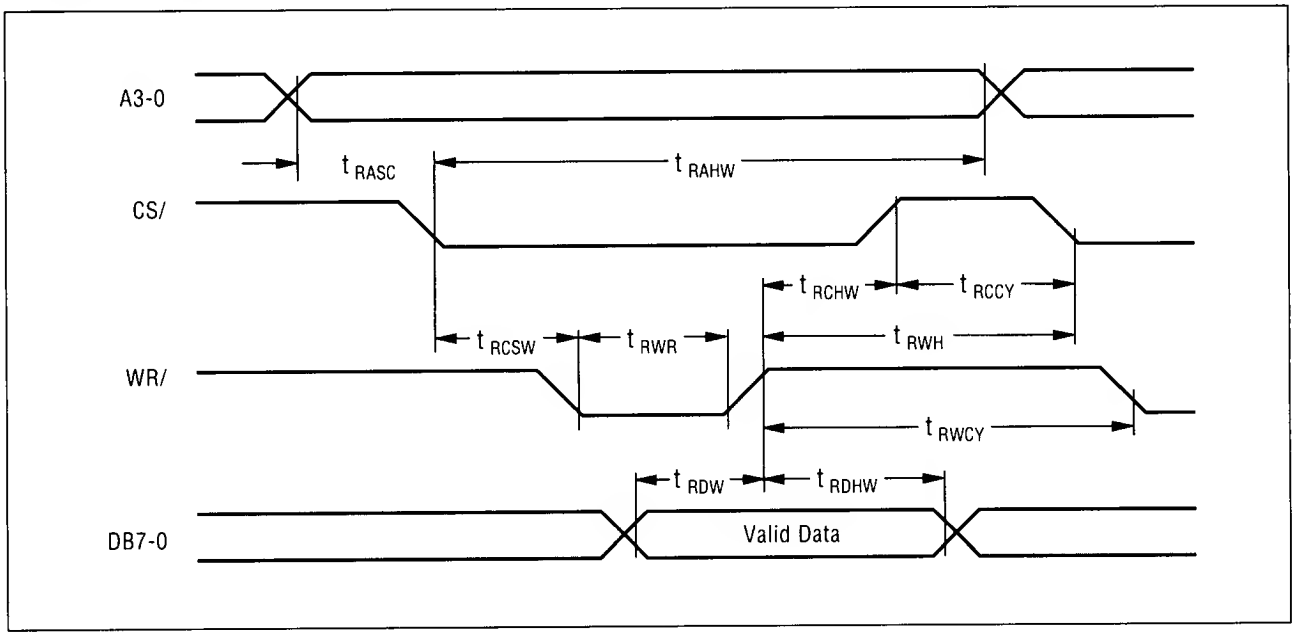


Parameter	Symbol	Minimum	Maximum	Units
INT/ to interrupt register RD/	t_{IR}	0	-	ns
RD/ pulse width	t_{RD}	50	-	ns
RD/ low to INT/ high	t_{RI}	-	100	ns
RD/ high to INT/ low	t_{ICY}	t_{CS}	-	ns

1) Refer to the register read specification for the timing require-ment of CS/, RD/, and A3-A0 for reading the interrupt status register.

2) The interrupt status register should not be read when INT/ is inactive.

Register Write



Parameter	Symbol	53C90A Min	53C90A Max	53C90B Min	53C90B Max	Units
Address setup to CS/	t_{RASC}	0	-	0	-	ns
CS/ setup to WR/	t_{RCSW}	0	-	0	-	ns
WR/ pulse width	t_{RWD}	40	-	40	-	ns
Data setup to WR/ high	t_{RDW}	15	-	15	-	ns
Address hold time from CS/	t_{RAHW}	50	-	50	-	ns
Data hold time from WR/	t_{RDHW}	0	-	0	-	ns
WR/ high to CS/ high	t_{RCHW}	0	-	50	-	ns
WR/ high to CS/ low	t_{RWH}	60	-	60	-	ns
CS/ high to CS/ low	t_{RCCY}	40	-	40	-	ns
WR/ high to WR/ low	t_{RWCY}	60	-	60	-	ns

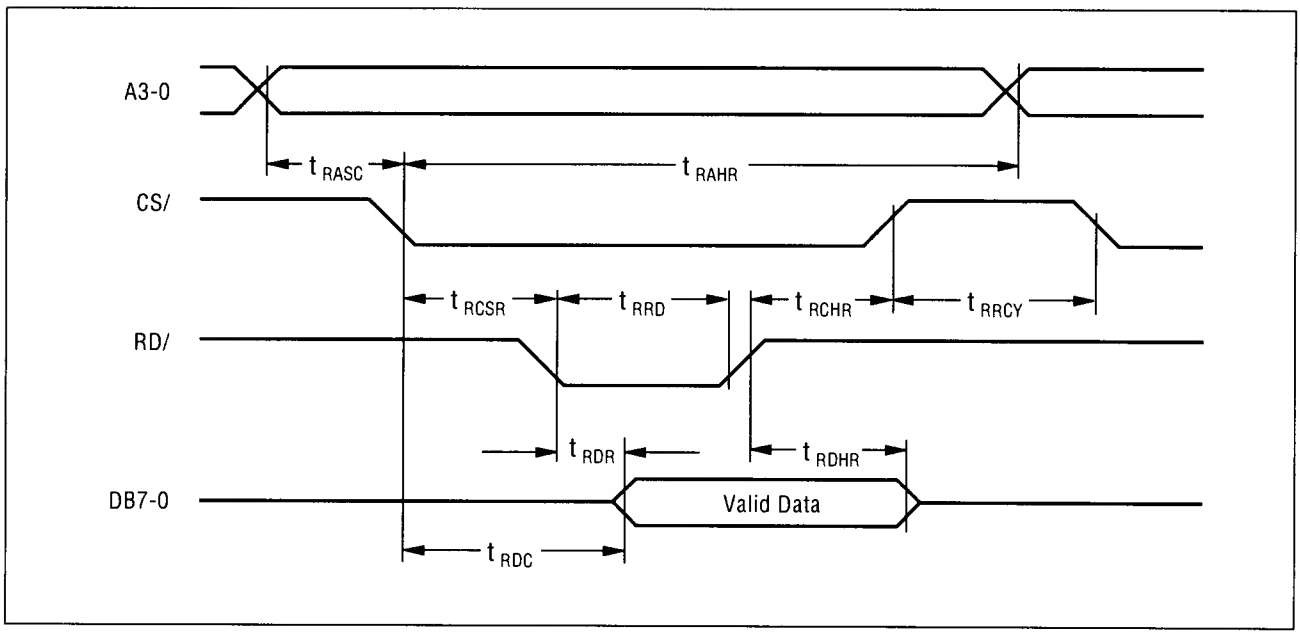
1) DACK/ must be inactive during all register I/O.

2) CS/ must be cycled to capture a new register address.

3) WR/ edges may precede or follow CS/ edges. If WR/ is held low, the data setup to CS/ high is 25 ns minimum, the data hold from CS/ high is 60 ns minimum and t_{RCCY} is 60 ns minimum.

4) t_{RCHW} may be reduced to zero on 53C90B if certain parity control options are not required. Refer to SEN 819.

Register Read



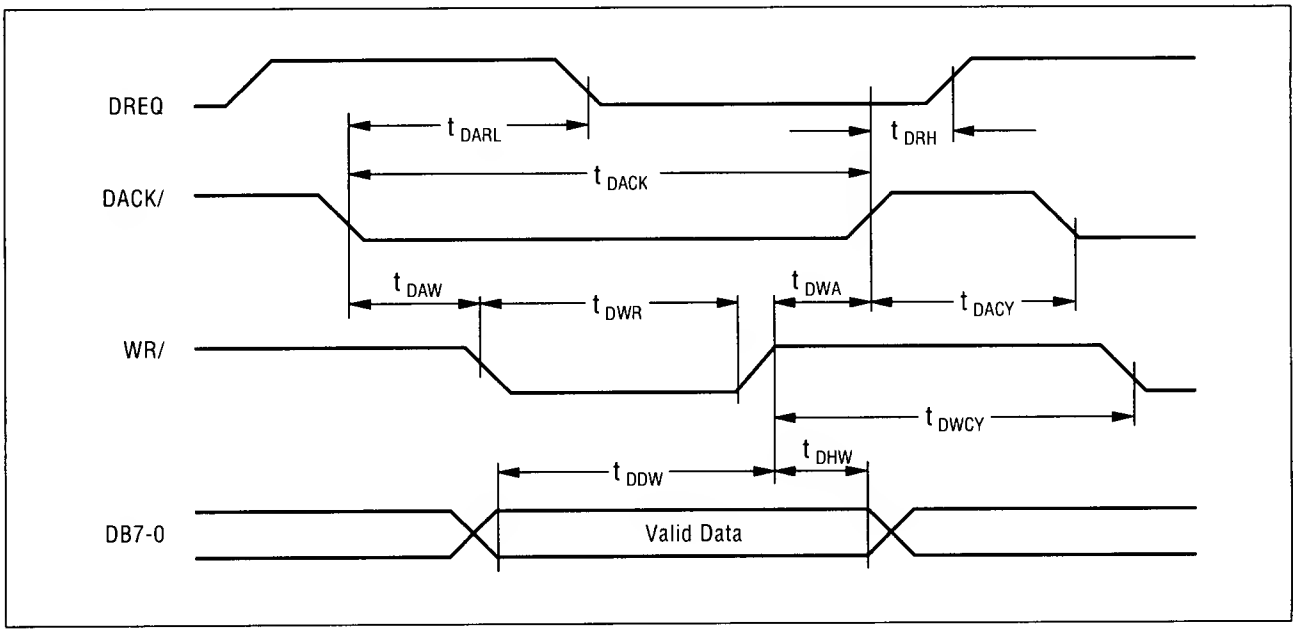
Parameter	Symbol	Minimum	Maximum	Units
Address setup to CS/	t_{RASC}	0	-	ns
CS/ setup to RD/	t_{RCSR}	0	-	ns
RD/ pulse width	t_{RRD}	50	-	ns
RD/ to data valid	t_{RDR}	-	50	ns
CS/ to data valid	t_{RDC}	-	70	ns
Address hold time from CS/	t_{RAHR}	50	-	ns
Data hold time	t_{RDHR}	2	40	ns
RD/ high to CS/ high	t_{RCHR}	0	-	ns
CS/ high to CS/ low	t_{RRCY}	40	-	ns

1) DACK/ must be inactive during all register I/O.

2) CS/ must be cycled to capture a new register address.

3) RD/ edges may precede or follow CS/ edges. If RD/ is held low, the time from CS/ low to stable data is t_{RDC} and the data release time from CS/ high is t_{RDHR}.

DMA Write



1) For synchronous data transfers DACK/ low to DACK/ high must equal or exceed $2t_{CP}$ and $t_{CS} + 35 - t_{DACY}$.

2) DREQ will remain true as long as the FIFO has room to receive at least one more byte. If the current write cycle fills the FIFO, DREQ will go false. If the SCSI bus the removes a byte from the FIFO, DREQ will not go true until DACK/ goes false.

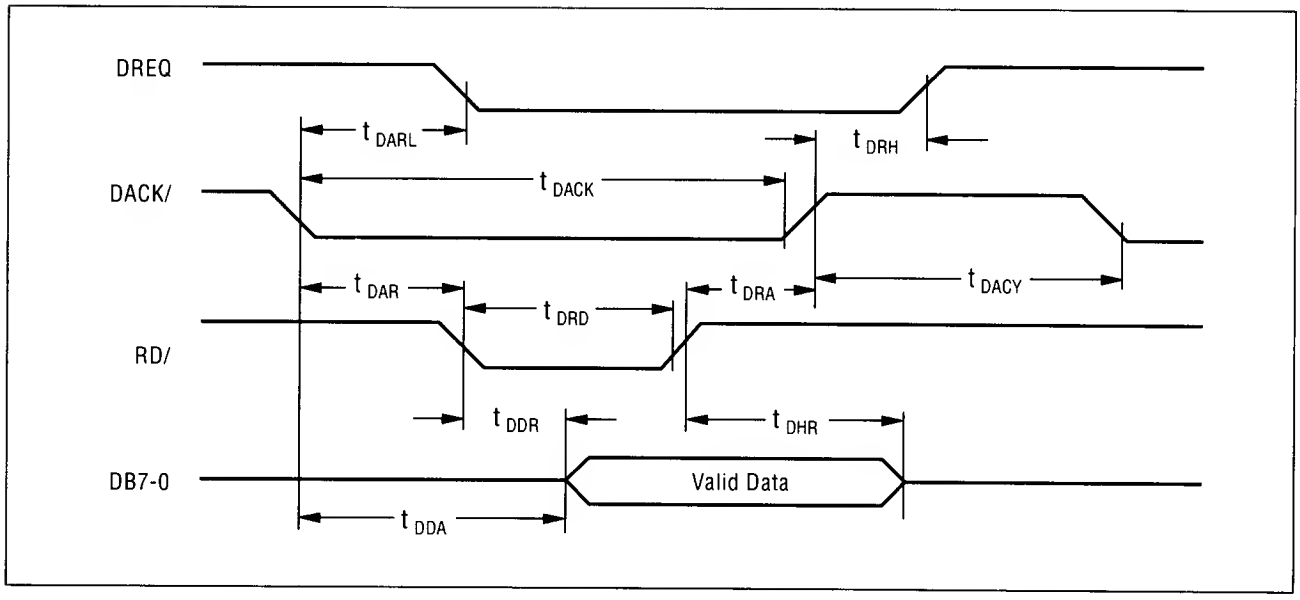
Parameter	Symbol	Minimum	Maximum	Units
DACK/ low to DREQ low (negation pending)	t_{DARL}	0	38	ns
DACK/ low to WR/ low	t_{DAW}	0	-	ns
WR/ pulse width	t_{DWR}	40	-	ns
Data to WR/ high	t_{DDW}	15	-	ns
WR/ high to DACK/ high	t_{DWA}	0	-	ns
Data hold time	t_{DHW}	0	-	ns
DACK/ high to DACK/ low	t_{DACY}	12	-	ns
DACK/ high to DREQ high (assertion pending)	t_{DRH}	0	50	ns
DACK/ pulse width	t_{DACK}	50	-	ns
WR/ high to WR/ low	t_{DWCY}	40	-	ns

1) CS/ must be inactive during all DMA accesses.

2) DACK/ must be cycled once for each read access.

3) WR/ edges may precede or follow DACK/ edges. If WR/ is held low, the data setup to DACK/ high is 15 ns minimun, and t_{DACY} is 40 ns minimum.

DMA Read



1) For synchronous data transfers DACK/ low to DACK/ high must equal or exceed $2t_{CP}$ and $t_{CS} + 35 - t_{DACY}$.

2) DREQ will remain true if there are more bytes in the FIFO. If the current read cycle empties the FIFO, DREQ will go false. If the SCSI bus then loads another byte into the FIFO, DREQ will not go true until DACK/ goes false.

Parameter	Symbol	Minimum	Maximum	Units
DACK/ low to DREQ low (negation pending)	t_{DARL}	0	38	ns
DACK/ low to RD/ low	t_{DAR}	0	-	ns
RD/ pulse width	t_{DRD}	50	-	ns
RD/ to data valid	t_{DDR}	-	41	ns
DACK/ high to data valid	t_{DDA}	-	60	ns
RD/ high to DACK/ high	t_{DRA}	0	-	ns
Data hold time	t_{DHR}	2	40	ns
DACK/ high to DACK/ low	t_{DACY}	12	-	ns
DACK/ high to DREQ high (assertion pending)	t_{DRH}	0	-	ns
DACK/ pulse width	t_{DACK}	50	-	ns

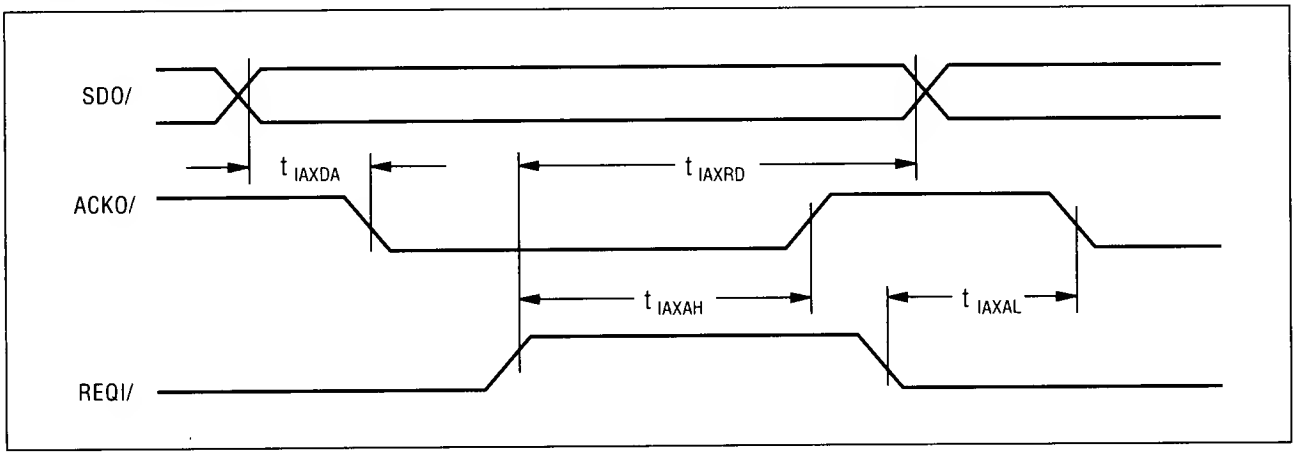
1) CS/ must be inactive during all DMA accesses.

2) DACK/ must be cycled once for each read access.

3) RD/ edges may precede or follow DACK/ edges. If RD/ is held low, the time from DACK/ low to stable data is t_{DDA} and the data release time is t_{DHR}.

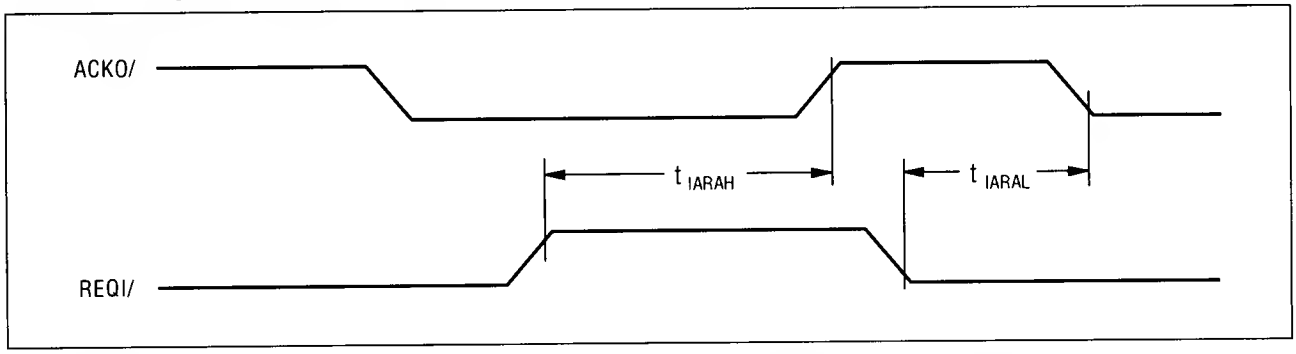
4) If $t_{DACY} \leq 15$ ns, then t_{DDA} is 45 ns max.

Initiator Asynchronous Send



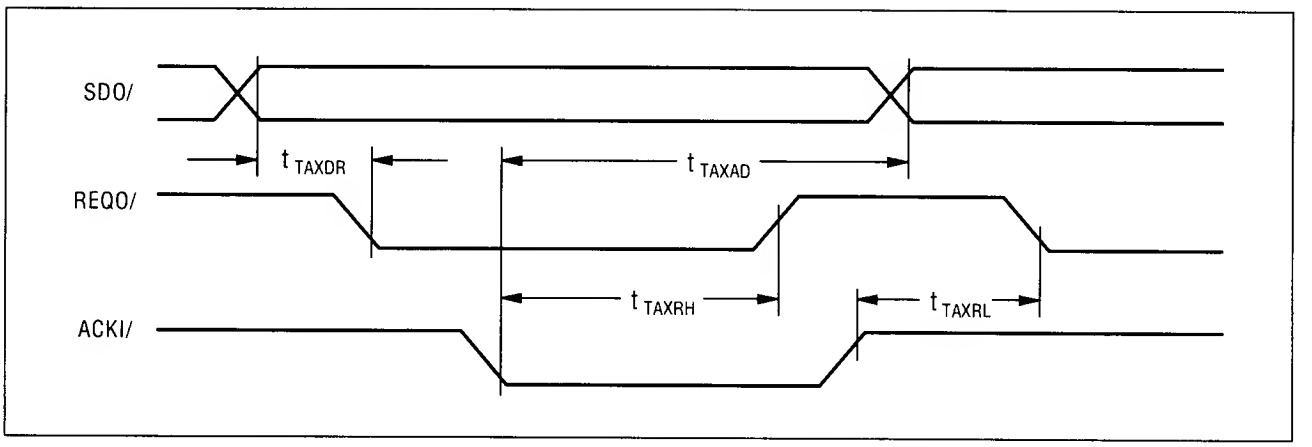
Parameter	Symbol	Minimum	Maximum	Units
Data to ACKO/ low	t_{IAXDA}	55	-	ns
REQI/ high to ACKO/ high	t_{IAXAH}	-	43	ns
REQI/ high to next data byte valid (FIFO bottom full)	t_{IAXRD}	-	75	ns
REQI/ low to ACKO/ low (Data already setup)	t_{IAXAL}	-	47	ns

Initiator Asynchronous Receive



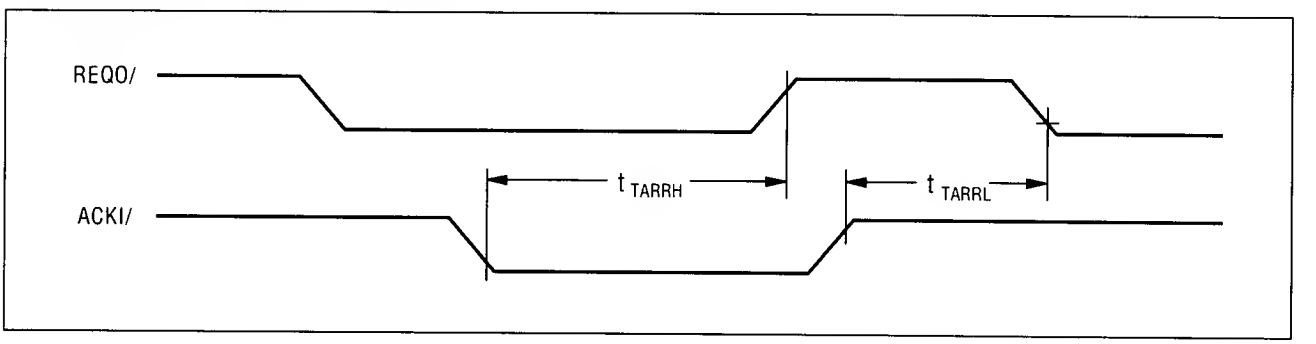
Parameter	Symbol	Minimum	Maximum	Units
REQI/ high to ACKO/ high	t_{IARAH}	-	43	ns
REQI/ low to ACKO/ low (FIFO not full)	t_{IARAL}	-	47	ns

Target Asynchronous Send



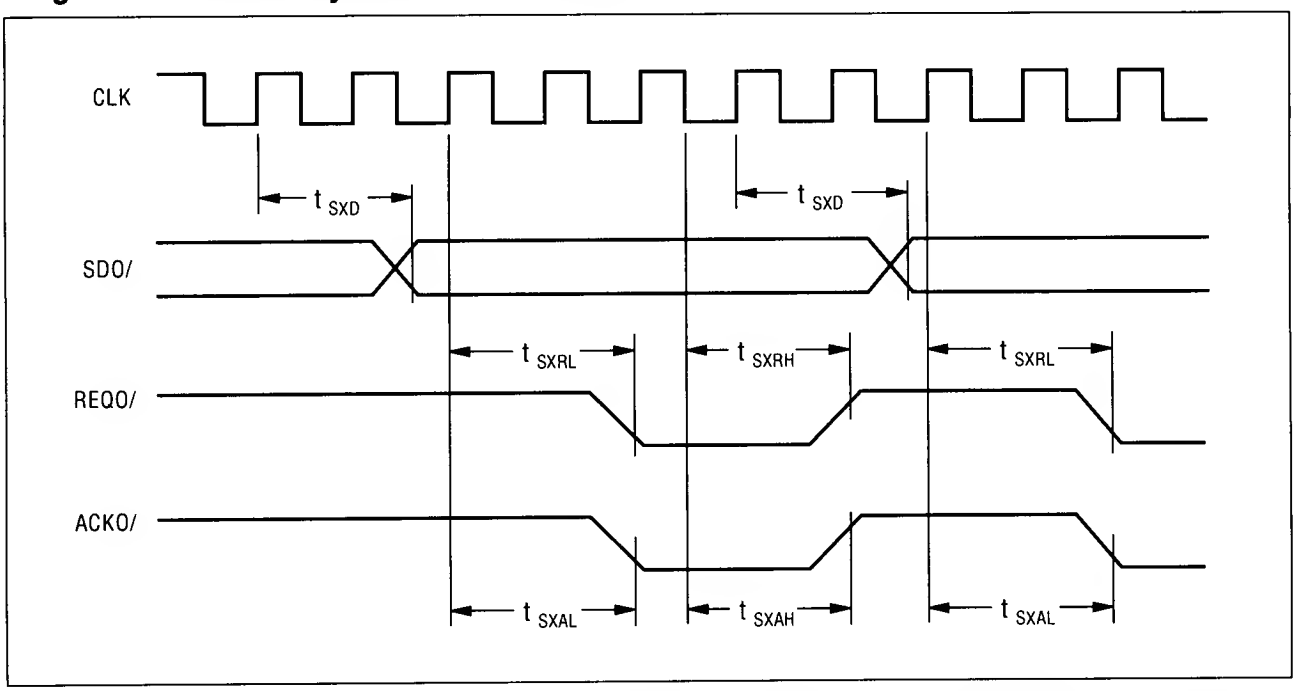
Parameter	Symbol	Minimum	Maximum	Units
Data setup to REQO/ low	t_{TAXDR}	55	-	ns
ACKI/ low to REQO/ high	t_{TAXRH}	-	43	ns
ACKI/ low to next data byte valid (FIFO bottom full)	t_{TAXAD}	-	78	ns
ACKI/ high to REQO/ low (data already setup)	t_{TAXRL}	-	45	ns

Target Asynchronous Receive



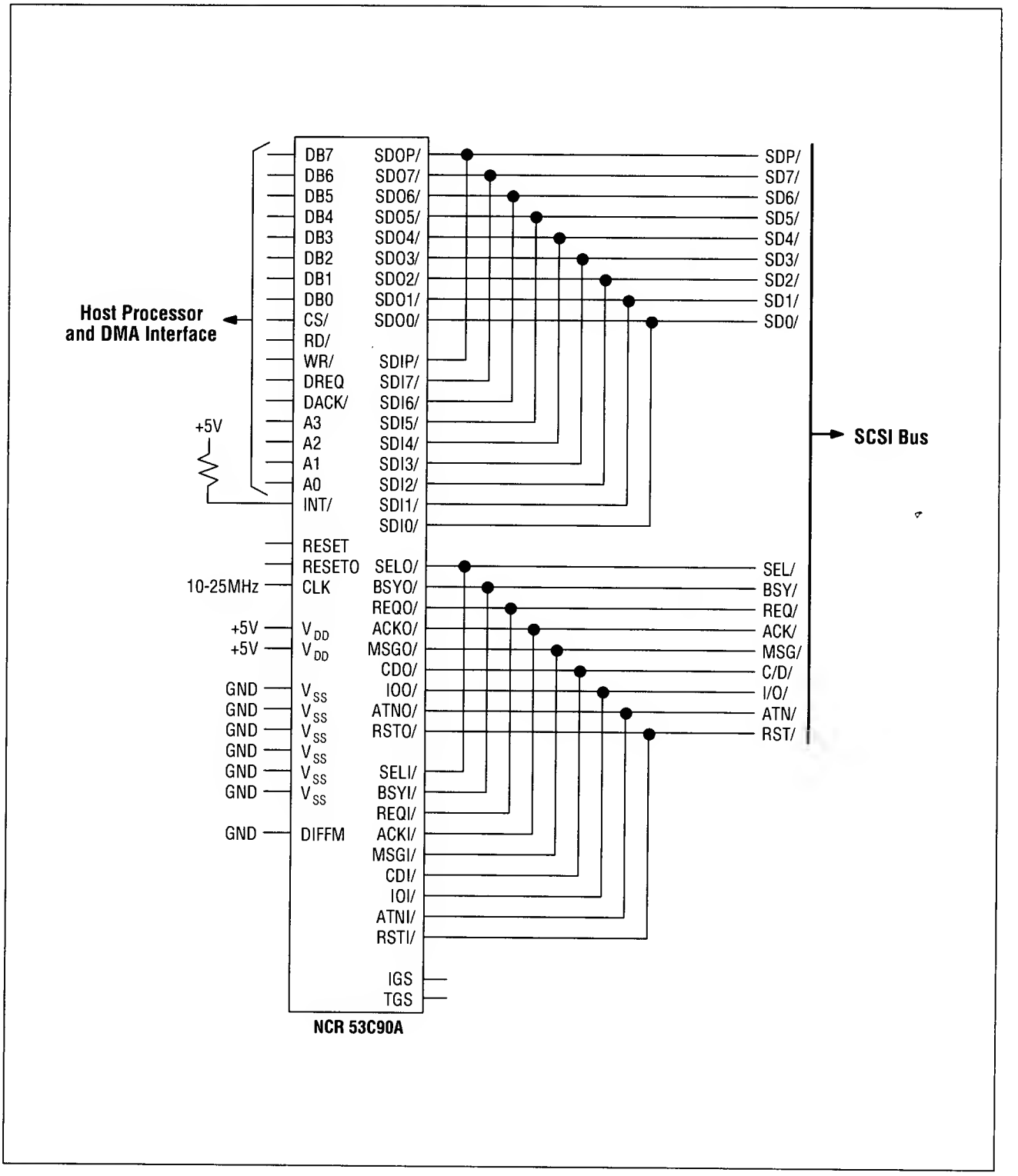
Parameter	Symbol	Minimum	Maximum	Units
ACKI/ low to REQO/ high	t_{TARRH}	-	43	ns
ACKI/ high to REQO/ low (FIFO not full)	t_{TARRL}	-	45	ns

Target and Initiator Synchronous Transmit

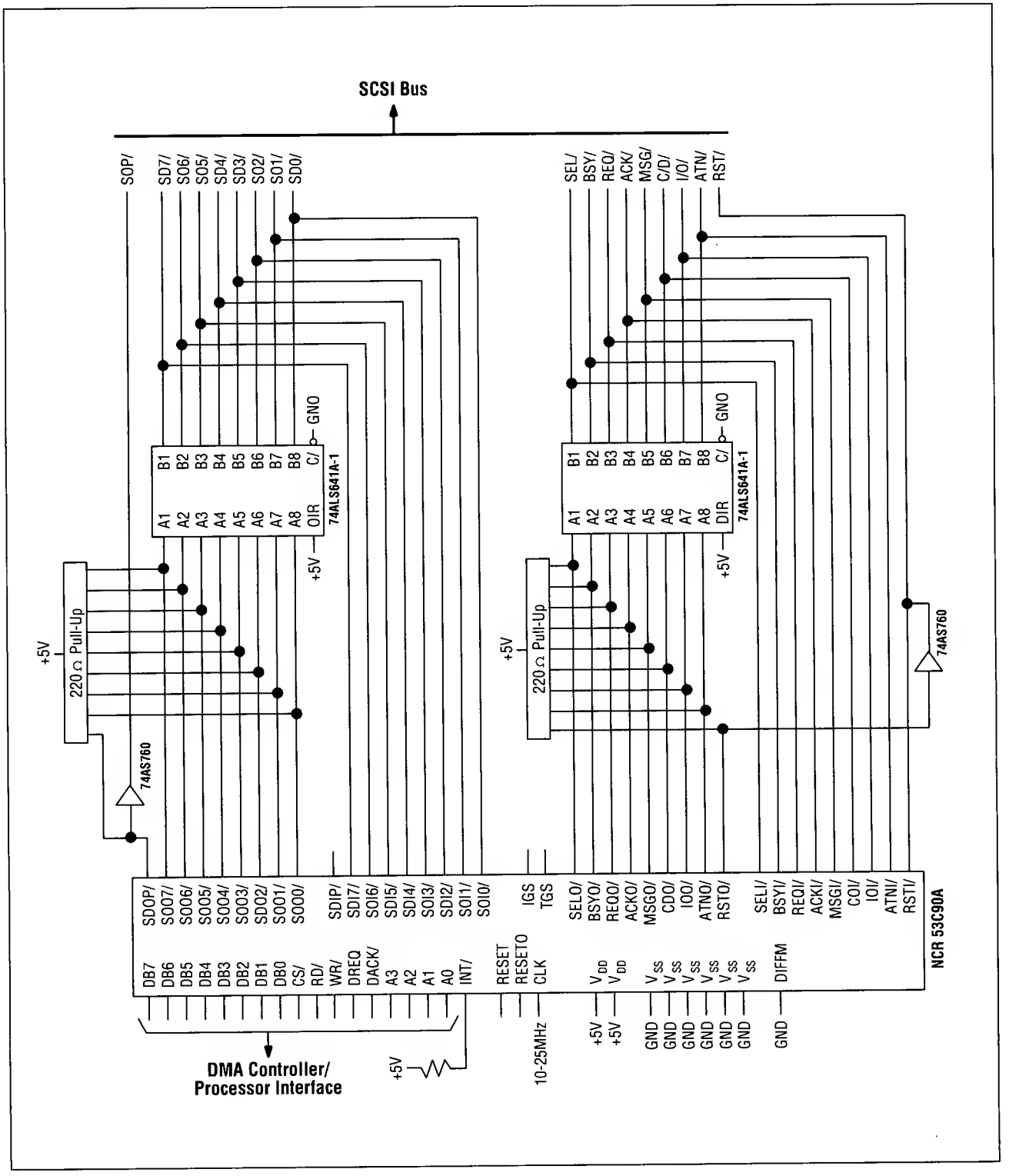


Parameter	Symbol	Minimum	Maximum	Units
Data from CLK high	t_{SXD}	-	90	ns
REQO/ low from CLK high	t_{SXRL}	-	70	ns
REQO/ high from CLK low	t_{SXRH}	-	68	ns
ACKO/ low from CLK high	t_{SXAL}	-	70	ns
ACKO/ high from CLK low	t_{SXAH}	-	68	ns

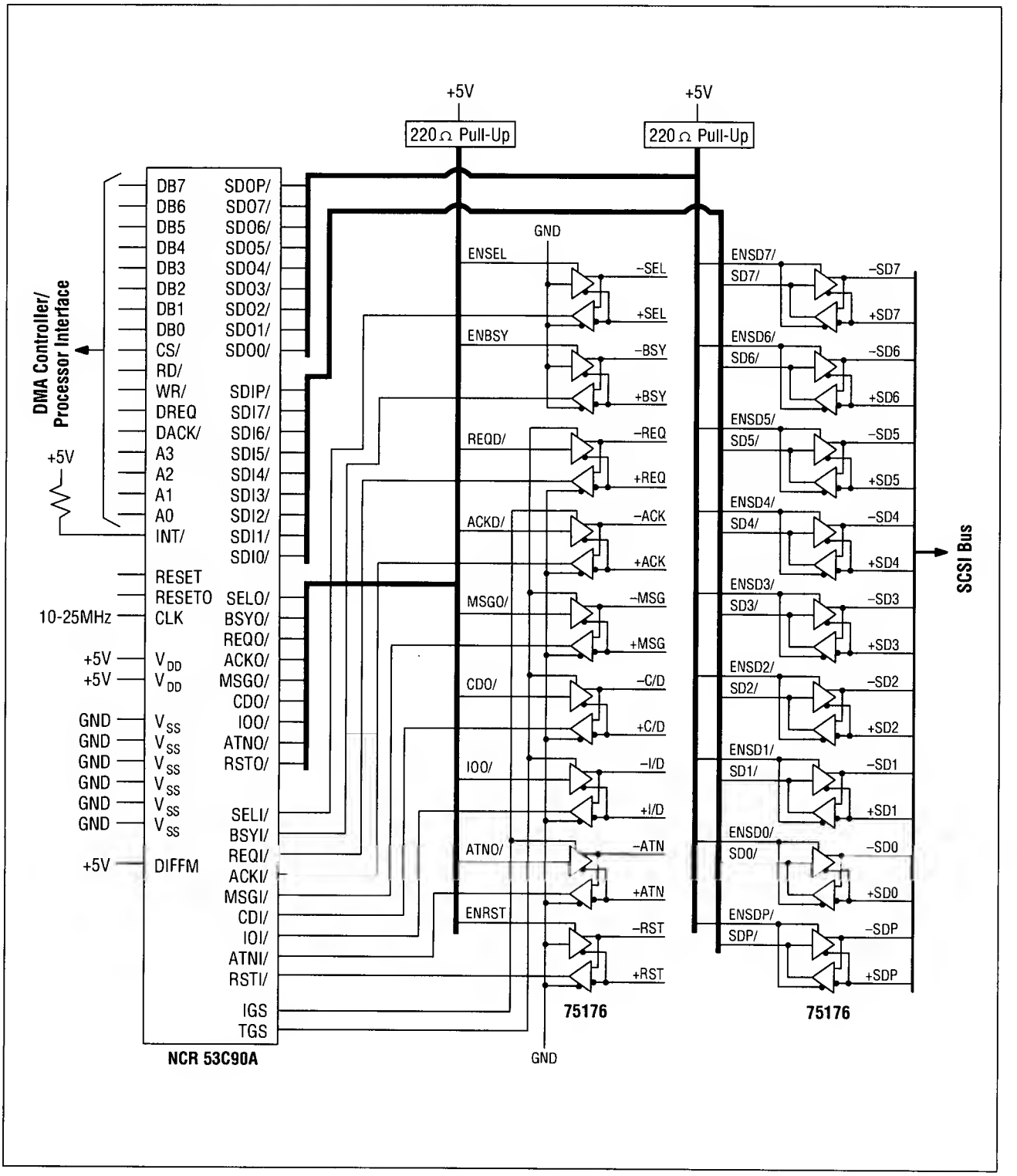
Single-Ended Mode without External Drivers



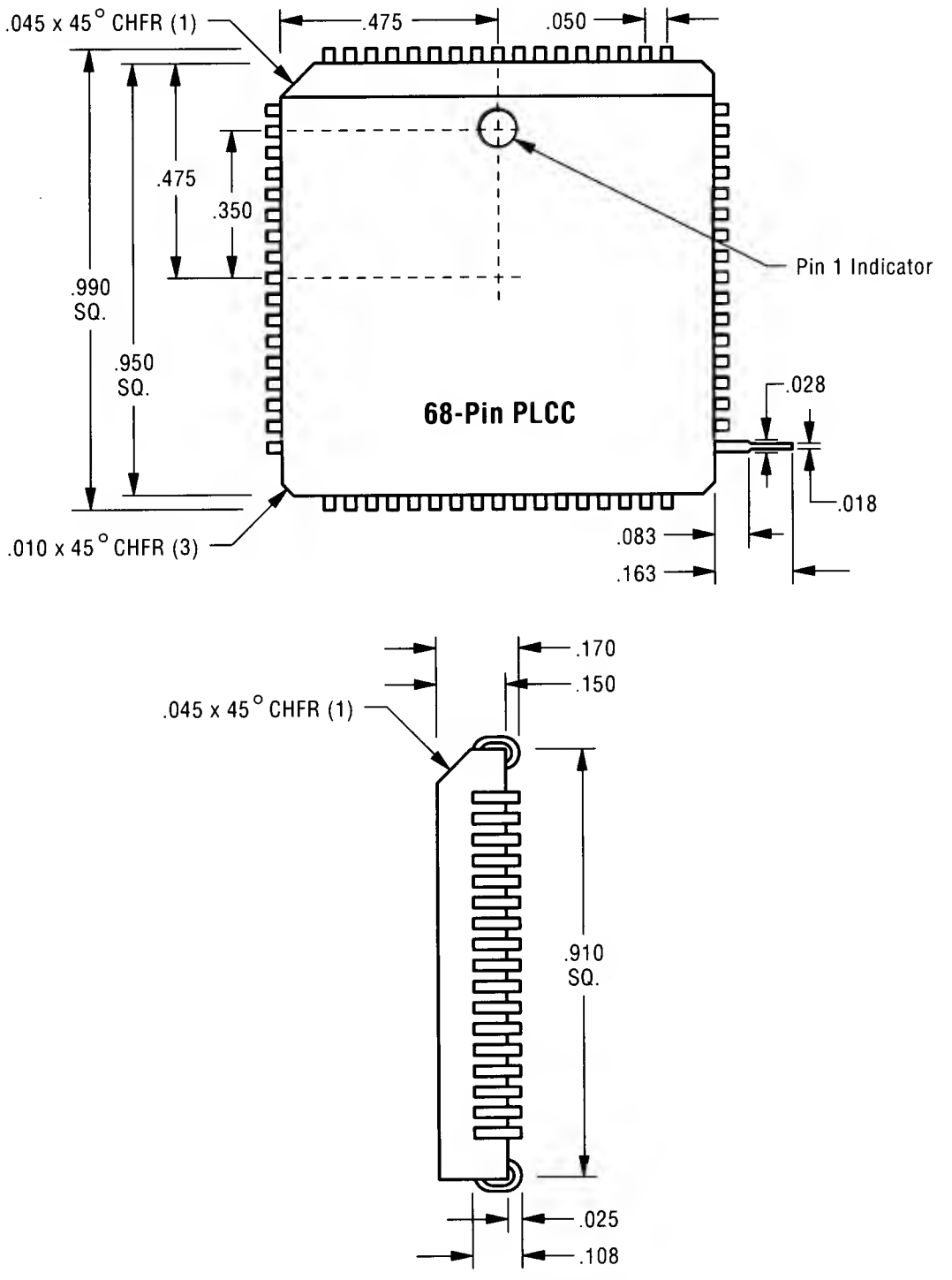
Single-Ended Mode without External Drivers (Continued)



Differential Mode

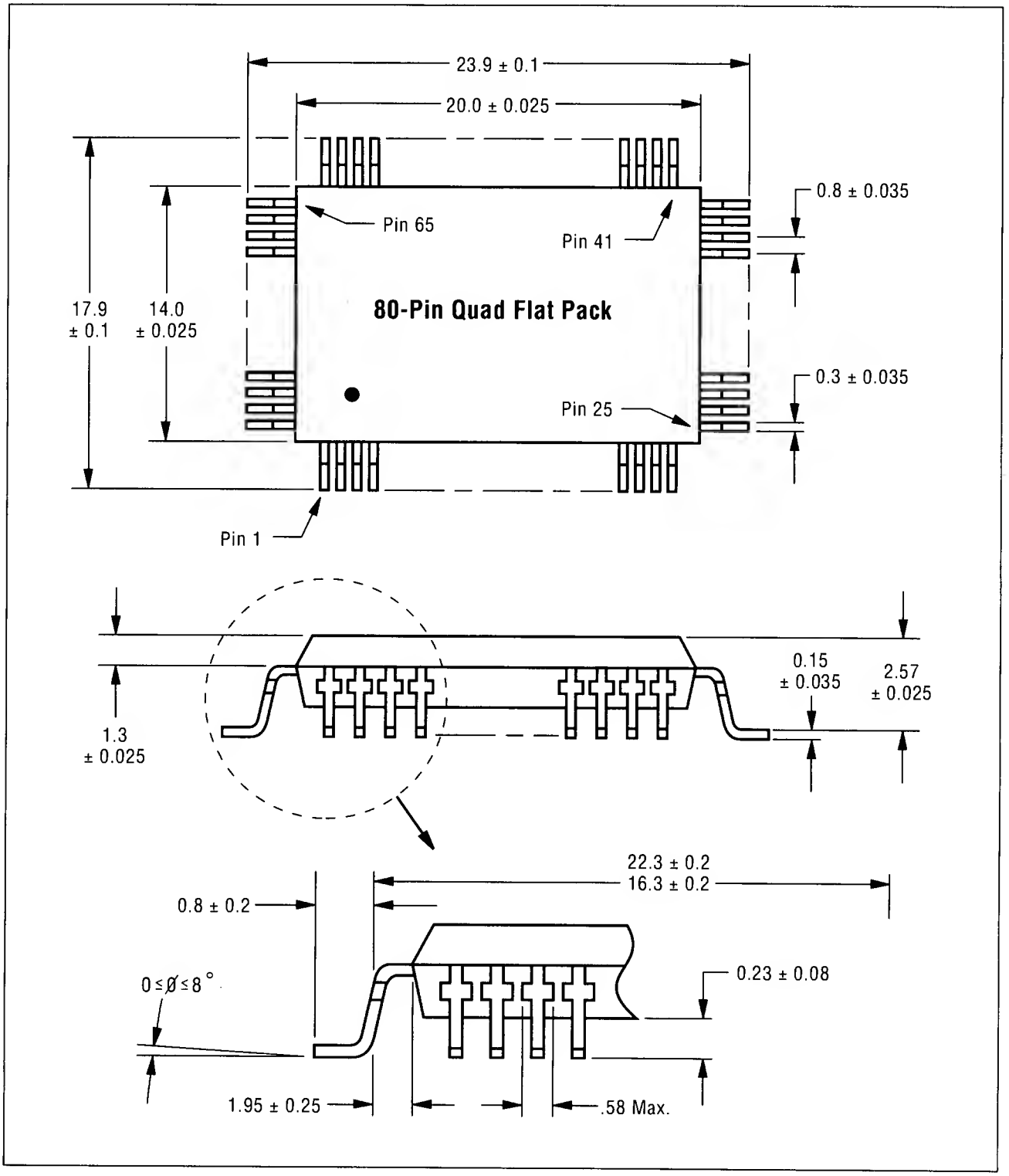


Mechanical Data



Note: *All dimensions are in inches*

Mechanical Data (Continued)



Note: All dimensions are in millimeters

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